THEORETICAL AND EXPERIMENTAL STUDIES OF BENDING/STRETCHING OF INORGANIC ELECTRONIC MATERIALS PRINTED ON PLASTIC SUBSTRATES AND THEIR PRACTICAL APPLICATIONS

BY

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DISSERTATION

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ABSTRACT

Flexible electronics based on inorganic devices has attracted increasing interest in versatile applications, from commercial systems, such as flat panel displays, to new possible systems, such as paperlike display, sensors, and medical devices, due to its many potential advantages including established electrical performance in comparison with organic based devices. However, the behavior of inorganic materials on plastic substrate by bending has been not studied well and the degree of bendability has simply defined by the bend radius at which the strain reaches some substantial fraction of a fracture strain (e.g., ~1 %) in a typical inorganic film. This thesis has been focused on the fundamental scientific studies necessary to establish the accurate bending induced mechanics of these systems and demonstration of various new inorganic based applications with high bendable and stretchable properties. Firstly, comprehensive experimental and theoretical studies of bending in flexible inorganic electronics on plastic substrates enable to understand the limits of flexibility and, moreover, improve this property of inorganic electronics on plastic substrate. Secondly, based on these studies, the focus of this thesis has been on the developments of highly bendable arrays of single crystalline silicon solar cells on plastic and highly bendable, stretchable, and deformable III-V compound semiconductor inorganic light emitting diodes (ILEDs) display as practical applications.

To my parents and family

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CHAPTER 1: INTRODUCTION

This chapter introduces an overview of my doctoral research about theoretical and experimental studies of bending/stretching of inorganic electronic materials printed on organic substrates and their practical approaches in flexible electronics. Section 1.1 introduces main motivation of this research. Section 1.2, in brief, introduces simple mechanics to calculate the strain of the device on the substrate on bending and discusses the limitation included in this model [1]. Section 1.3 describes implementations of these studies in practical approaches in flexible electronics. Significant components of Section 1.1 and 1.2 were published as S.-I. Park, J.-H. Ahn, X. Feng, S. Wang, Y. Huang, and J. A. Rogers, "Theoretical and experimental studies of bending of inorganic electronic materials on plastic substrates," *Advanced Functional Materials* **2008**, *18*, 2673-2684 [2] and refer to a paper published in *applied physics letter* in an article by Z. Suo *et al.* [1]. Significant components of Section 1.3 were published as S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K.-C. Hwang, P. Ferreira, X. Li, K. Choquette, and J. A. Rogers, "Printed Assemblies of Ultrathin, Microscale Inorganic Light Emitting Diodes for Deformable and Semitransparent Displays," *Science* **2009**, *325*, 977-981 [3].

1.1 Research Motivation

Interest in large-area electronics, sometimes referred to as macroelectronics, has experienced rapid growth in the last decade due to its significance in established systems such as liquid crystal displays (LCDs) and organic light emitting diodes (OLEDs)

displays. More recently, the field of macroelectronics has been extended in other, new applications, such as sensors, medical devices, and photovoltaics, which enable to distribute electronic functionality over sizes that are much larger than those associated with semiconductor wafers [4]. For many of these systems, various plastic or steel sheets with thin and lightweight properties represent ideal substrates. Therefore, various prototype flexible electronic devices, from paperlike displays [5] to sensor skins [6], have been demonstrated on these substrates, most commonly by use of semiconductors based on small molecule or polymer organics [7-10]. These classes of materials are generally believed to be well suited for these applications because they are themselves considered, in a very loose sense, to be 'flexible' and naturally compatible with plastic substrates. However, their critical weaknesses are that the electrical properties, such as the effective mobilities, on/off ratio, and the power consumption and the reliability of devices, such as the lifetime, formed with them are much worse than those of inorganic materials. Inorganic electronic materials, which have already applied in various electronic commercial products, have been developed and established with robust electric properties and long lifetime. These considerations have recently led to interest in the possibility of inorganic based flexible electronics [11-19], in which only the substrates or other passive elements (e.g., dielectrics) are organic. The most basic realization uses thin films of the inorganics as semiconductors, conductors and/or insulators on substrates that are also thin, to minimize the strains induced by bending [20,21]. In such designs, the electric properties and the reliability can be significantly improved without loss of bending properties in flexible electronics. Recently, these designs have reported bend radii of ~1 cm on plastic substrates [22] that have thicknesses in the 25-150 μm range, even without

advanced designs that use concepts of neutral mechanical planes [23-25] or buckled material configurations [26].

However, inorganic electronic materials have some issues, such as high temperature processing, bulky and heavy designs, and expensive material cost, that get over to apply in flexible large-area electronics. These issues are solved by the following strategies. (1) The plastic substrates limit maximum processing temperature to prevent their deformation. Therefore, low temperature processing or separation of high temperature processing from the substrates is necessary to apply inorganic materials on the plastic substrates. (2) Inorganic devices, which are commercially provided, have bulky, heavy, and incompact design (i.e. ~ a few hundreds μm, width × length × height) due to the limitation of processing, such as wafer sawing, serial pick&place, and wire bonding. The devices with thin and small sizes are required to achieve high bendability. New technologies, such as a transfer printing which is core technology to generate the devices including these properties, provide the answer to overcome the limitation of current inorganic devices. (3) While macroelectronics means large-area electronics, the inorganic semiconductors occupy pretty small area in entire area. Therefore, the registration of the semiconductor in exact position can dramatically reduce the consumption of these materials. Transfer printing method of the inorganic materials from the source wafer to the plastic substrate enables to register these semiconducting materials to suitable position without losing the meterials.

Inorganic electronics printed on plastic substrates are able to be a breakthrough not to lose both of properties, high electric performance and high flexibility, in flexible electronics. For this, analysis of the strain distribution is important to realize high

flexibility without any failure of materials. Therefore, failure mechanism of inorganic materials on plastics provides the understanding of the limitation of flexibility and, moreover, advanced design which can achieve enhanced robustness on bending.

In my doctoral research, the primary goals are to approach the fundamental scientific knowledge necessary to establish the accurate bending induced mechanics of these systems and to achieve various new inorganic electronic applications with high bendability. Firstly, comprehensive experimental and theoretical studies of bending in flexible inorganic electronics on plastic substrates enable to understand the limits of flexibility and, moreover, improve this property of inorganic electronics on plastic substrate. Secondly, based on these studies, my research is focused on the developments of highly bendable arrays of silicon solar cells on plastic and highly bendable, stretchable, and deformable inorganic light emitting diodes (ILEDs) display as practical approaches.

1.2 Theoretical Study of Bending

This section introduces simple, basic theory to calculate the strain of the device on the substrate under bending condition [1] and a necessity of advanced mechanical modeling which is interconnect with the motivation of my doctoral research.

In flexible inorganic electronics the strain at the top surface of the device substrate is approximated by [1]

$$\varepsilon_{top} = \left(\frac{h_s + h_f}{2R}\right)\frac{(1+2\eta+\chi\eta^2)}{(1+\eta)(1+\chi\eta)}, \quad (1)$$

where h_f, h_s, R, η, and χ denote the film thickness, the substrate thickness, the bend radius, h_f / h_s, and the ratio of Young's modulus of the film and the substrate (Y_f / Y_s),

respectively. However, equation (1) are still far too simple to provide either an accurate description of the mechanics or a predictive framework for understanding different modes of bending induced failure in these structures because the degree of bendability is defined by the bend radius at which the strain reaches some substantial fraction of a fracture strain in a typical inorganic film (e.g., ~1%). Different from previous mechanics models [1], the analysis of bending strain in my doctoral research does not assume the thin film to cover the entire substrate, thereby explicitly accounting for effects of edges and finite device sizes, both of which play critically important roles in the mechanics and bending properties [2]. These thin-film islands give non-uniform stress, with maxima that often appear at the edges and spatially non-uniform shear and normal stresses along the film substrate interface [2]. These results are generally applicable to all classes of flexible inorganic electronics on plastic substrates. The observations and analysis explain all of the different failure mechanisms in unoptimized systems; they also rationalize the key mechanisms by which somewhat more advanced layouts can achieve enhanced robustness on bending.

1.3 Practical Approaches in Photovoltaic and Optoelectronic Systems

Based on transfer printing techniques of inorganic materials on foreign substrates, highly bendable arrays of simple silicon (Si) p-n junction diodes (Chap. 2) and more complicated single crystalline Si solar cells (Chap. 4) demonstrate these experimental and theoretical studies (Chap. 2, 3) in practical flexible inorganic devices. The transfer printing techniques enable to retrieve much thinner and smaller inorganic materials in comparison with other process technologies [27,28]. Therefore, the small sizes of the Si

diodes and the room-temperature schemes for integrating them into modules enable the use of thin, lightweight flexible substrates for ease of transport and installation.

The other implementation of these studies is highly deformable and bendable inorganic light-emitting diodes (ILEDs) display (Chap. 5). Organic light-emitting diodes (OLEDs) display is rapidly emerging as an attractive alternative to liquid crystal displays (LCDs) due to their comparatively high refresh rates, contrast ratios, power efficiencies and capacity for vibrant color rendering [29,30]. ILEDs can also form displays, with properties such as brightness, lifetime and efficiency that can exceed those possible with OLEDs [31,32]. However, these displays exist only in ultra-large area, low resolution formats limited by processing and assembly procedures that do not scale effectively to small (< ~200x200 μm), thin (< ~200 μm) light emitters or to dense, high pixel count arrays. An ability to replace existing methods for fabricating ILEDs (i.e. wafer sawing, serial pick-and-place, wire bonding and packaging on a device-by-device basis) and for incorporating them into displays (i.e. robotic assembly into tiles followed by interconnection using large quantities of bulk wiring) with those that more closely resemble the planar, batch processing of OLEDs would greatly expand the application opportunities. Examples include not only ILED displays for desktop monitors, home theater systems and instrumentation gauging, but also, when implemented in flexible or stretchable forms, wearable health monitors or diagnostics and biomedical imaging devices. In microscale sizes, such ILEDs can also yield semitransparent displays, with bidirectional emission characteristics, for vehicle navigation, heads-up displays and related uses. The strategy involves four key components: (1) epitaxial semiconductor multilayers designed for lateral delineation and release from a source wafer to yield

isolated arrays of ILEDs, each of which remains tethered to the wafer by polymeric 'breakaway' anchor structures; (2) printing techniques for manipulating the resulting ILEDs in schemes that enable formation of large scale arrays on foreign substrates and in arbitrary spatial layouts; (3) planar processing methods for establishing electrical interconnects to the devices, in direct or matrix addressable configurations; and (4) integration strategies capable of yielding ILED displays in flexible or stretchable formats, and with conventional, semitransparent and bidirectional emitting characteristics. Certain aspects build on previously reported procedures for etching and manipulating epitaxial semiconductor layer [33-39] and for fabricating flexible and stretchable electronics [40,41]. Based on these strategies and experimental/theoretical fundamental studies, ILEDs lighting/display systems can establish highly deformable and bendable performance.

1.4 In This Thesis

This thesis is organized into four major sections: experimental studies of bending in single crystalline silicon ribbons on plastic (Chap. 2), theoretical studies of bending mechanics of inorganic electronic materials on plastic (Chap. 3), practical approaches in silicon photovoltaics (Chap. 4), and practical approaches in III-V ILEDs optoelectric systems (Chap. 5).

- In Chap. 2, failure mechanisms of inorganic materials on plastic substrates are described. Cracking, slipping, and delaminating of inorganic materials are experimentally observed.

- In Chap. 3, theoretical analysis of above failure mechanisms are studied by non-uniform stress, with maxima that often appear at the edges and spatially non-uniform shear and normal stresses along the film/substrate interface.
- In Chap. 4, highly bendable arrays of simple silicon p-n junction diodes and more complicated monocrystralline silicon solar cells are demonstrated.
- In Chap. 5 and App. A, highly bendable, foldable, and deformable ILEDs displays are demonstrated and related light emission characteristics and mechanics are studied.
- In Chap. 6, all of doctoral research works are summarized.

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CHAPTER 2: EXPERIMENTAL STUDIES OF BENDING IN SINGLE CRYSTALLINE SILICON RIBBONS ON PLASTIC

This chapter describes materials and mechanics aspects of bending, which are experimentally observed, in systems consisting of ribbons and bars of single crystalline silicon (Si) printed on plastic substrates. Section 2.1 and 2.2 describe experimental methods to fabricate the Si ribbons on plastic substrates and observation of different failure modes depending on their thicknesses. Section 2.3 presents a length effect of the Si ribbons on plastic substrates. Section 2.4 introduces the other implementations to improve the flexibility, such as encapsulation and neutral mechanical plane schemes. Significant components of chapter 2 were published as S.-I. Park, J.-H. Ahn, X. Feng, S. Wang, Y. Huang, and J. A. Rogers, "Theoretical and experimental studies of bending of inorganic electronic materials on plastic substrates," *Advanced Functional Materials* **2008**, *18*, 2673-2684 [1].

2.1 Experiment

This section describes methods for fabrication of microscale single crystalline Si ribbons on plastic substrates and for bending test to investigate the failure modes of these inorganic materials.

2.1.1 Fabrication of Si Ribbons on Plastic Substrates

Figure 2.1 schematically illustrates the processing steps for creating and transferring thin ribbons of silicon from a source wafer to a plastic substrate and the types

of bending tests that were performed. The layouts were designed explicitly to reveal the key aspects of the mechanics and the various possible failure modes. They are not intended for practical use in flexible electronics; subsequent sections describe multilayer structures that are more suitable for this purpose.

The first step involved the definition of Si ribbons from a silicon-on-insulator (SOI) wafer, using SF_6 reactive ion etching (RIE) through a patterned layer of photoresist. Photoresist (PR; AZ 5214, 3000 rpm, 30s) was coated on a silicon-on-insulator (SOI) wafer (Soitec or Shin-Etsu) and baked at $110\,^{o}C$ for 1 min. This layer of PR was then photolithographically exposed (10 $mWcm^{-2}$, 12 sec, Karl Suss MJB3 mask aligner) and developed (AZ 327 MIF developer, 45 s) to define the layouts of the Si ribbons. Dry etching using SF_6 reactive gas (Plasma-Therm reactive ion etching (RIE) system, 40 sccm, 50 mTorr, 100 W) through the PR etched the exposed silicon to expose the buried oxide. In the case of thick (i.e., 10 μm) Si, SOI wafers with 10 μm thick top Si layer were etched with a SF_6/O_2 inductively coupled plasma reactive ion etching system (STS-ICPRIE, STS Mesc Multiplex Advanced Silicon Etcher) through a patterned layer of Si_3N_4/SiO_2 (3/30 nm), as a hard mask, grown by plasma enhanced chemical vapor deposition (PECVD, Plasma-Therm) and patterned by photolithography and etching [2].

Removal of the resist layers followed by undercut etching of the buried oxide released arrays of Si ribbons, without physically lifting them off of the wafer. The undercut etching of the buried oxide was performed with concentrated hydrofluoric (HF) acid solution (~49 wt % in water). The hard mask for the 10 μm thick Si layer was also removed by HF. The Si ribbons sagged to bottom Si handle wafer at the end of of this etching process.

In the next step, to pick the ribbons up from the wafer, a flat elastomeric stamp of polydimethylsiloxane (PDMS) (Sylgard 184, Dow Corning) contacted the Si ribbons on the wafer after blow drying with N_2 gas. The ribbons adhered to PDMS by Van der Waals interactions (Fig. 2.1a). Efficient transfer of the ribbons from the substrate to the PDMS was accomplished by peeling back the stamp at a relatively high speed (Fig. 2.1b) [2-4].

Contacting the stamp, coated with ribbons in this manner, against a poly(ethyleneterepthalate) (PET) (50 μm or 175 μm thick) substrate coated with a thin epoxy adhesive layer (~1 μm thick) and then removing the stamp completed the transfer process. In all experiments presented in this chapter, this epoxy (SU8, Microchem) was spin-coated (75% diluted solution, 3000 rpm, 40s), soft baked at 65^oC and 110^oC for 1 min each, exposed to ultraviolet (UV) light (10 $mWcm^{-2}$, 12 sec) and then postbaked at 115^oC for 1.5 min to induce cross-linking before the transfer process. Removal of the stamp was performed at slow speeds by use of heating (110^oC, 1.5 min), to induce thermal expansion in the PDMS and, in this way, to initiate separation of the PDMS stamp and the ribbons (Fig. 5.1c). After the transfer process, the Si/epoxy/PET substrate was heated, in a final step, to eliminate the solvent and complete the cure of the epoxy at 110^oC for 13.5 min. This configuration results in the ribbons resting on the surface of the epoxy, but neither embedded in it or directly chemically bonded.

2.1.2 Bending Test

The bending properties, including the failure modes, were investigated using a home-built set of translation stages and fixtures capable of mounting directly in a

scanning electron microscope (SEM, Philips XL30 ESEM-FEG, at low operating voltages of 1 keV to avoid damage to the sample or other changes induced by heating from the electron beam) at tilt angles (outward bending: 38.5°, inward bending: ~30°) for viewing during the bending process. Three different failure modes were observed, depending on the sample type: cracking of the silicon, slipping of the silicon along the interface with the epoxy and delamination of the silicon from the epoxy. Figure 2.1d schematically illustrates these modes. The extent of bending necessary to induce failure and the mode for failure depend on the thickness and other dimensions of the silicon, the nature of the adhesive and the thickness of the substrate.

The measurements were performed with the ribbons on substrates with initial lengths L, subject to compression with external force applied through the bending stage (Fig. 5.1c). Figure 5.1d shows the plastic substrate bent to an end-to-end length of L-dL (i.e., horizontal distance from one edge of the bent substrate to the other). The setups allow the length to be measured with an accuracy better than ~0.1 mm, and continuous control of L-dL, in increments of ~0.1 mm. The experimentally measured L and L-dL can be used to compute the approximate, nominal bend radius (R_{nom}) defined near the center of the length of the substrate. This quantity is given by the reciprocal of the curvature of substrate as computed from the second derivative of the sinusoidal curve that describes the bent shape $w = w_0 \sin\left(\pi X / L\right)$, where

$$w_0 = \frac{2}{\pi} L \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12 L^2}} \quad [5], \tag{1}$$

and dL / L, h_s, w, and w_0 denote the applied strain, the substrate thickness, the deflection of the substrate in the z direction, and the deflection of the substrate at the

center (i.e., $X=L/2$), respectively. This analysis applies to the experimental configuration, in which the ends of the substrate are free to rotate upon bending (i.e., they are unclamped). This bend radius, given by

$$R_{nom} = \frac{L}{2\pi\sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12L^2}}} \tag{2}$$

is an approximate, global value that does not include the mechanical effects of the silicon. A corresponding, nominal bending strain, ε_{nom}, is also defined as $h_s/(2R_{nom})$ [6].

2.2 Failure Modes: Cracking, Slipping, and Delamination

This section reports different failure modes observed by SEM (Philips XL30 ESEM-FEG) on bending, depending on the thickness of the Si ribbons on plastic substrate coated with adhesive layer.

Figure 2.2 shows SEM images of the Si ribbons with 100 nm thickness, 20 μm widths 500 μm lengths on a PET sheet (175 μm thick) with length L=11.8 mm, coated with an epoxy adhesive layer (~1 μm thick). These images show that in this system, as well as the others used to illustrate the mechanics concepts, the silicon rests primarily on the top surface of the adhesive, yielding a configuration that is not well suited to strong bonding to the substrate. As mentioned in section 2.1, this type of layout was chosen to study because it reveals clearly all of the relevant mechanical behaviors and failure modes. The left insets schematically illustrate the bending geometries. The results show that bending induced failure in this case occurs when cracks appear in the silicon. Cracks are first visible at dL/L= 42.4 % (R_{nom} ~2.88 mm, ε_{nom} ~3.04 %). The cracks form near the centers of the ribbons, and originate from single fracture lines that run across the ribbons

and propagate through different paths resulting in many fractured pieces at values of strain (dL/L = 45.8 %) larger than the failure threshold (Fig. 2.2b). The right inset of Figure 2.2b provides a magnified view of a cracked region.

As expected, the thickness of the ribbons plays an important role in the mechanics. To illustrate the effects, Figure 2.3 shows SEM images of the edges of silicon ribbons with 700 nm thicknesses in designs that are otherwise similar to those of Figure 2.2, except that a 50 μm thick PET substrate (L=11.8 mm) was used to achieve dL/L values at failure that are convenient for measurement. In this case, instead of cracking, the ribbons were slipped on the substrate at dL/L = 9.0 % (R_{nom} ~6.26 mm, ε_{nom} ~0.40 %,), as shown in Figure 2.3a. Figure 3a–c shows that the Si ribbons slip by progressively increasing amounts as dL/L increases [a) 9.0 %, b) 31.4 %, and c) 50.8 %]. This slipping reduces the strain in the silicon, thereby preventing the cracking failure mode even at extremely high values of dL/L. As the bending is released, the silicon ribbons often do not slip back to their original locations but instead buckle upward via local delamination from the adhesive, in a manner that foreshadows the third failure mode. This slipping result shows clearly an example of a system in which degree of bendability is not determined simply by the fracture strains of inorganic electronic materials. Instead, interfacial shear stresses (τ), which are responsible for the slipping behavior, determine failure. These shear stresses have maximum values near the free edges of the silicon. Unlike fracture, which is limited by the failure strain of the silicon, this failure mode is extremely sensitive to the strength of adhesive bonding to the substrate. Details of theoretical analysis for this failure mode will be discussed in chapter 3.

Increasing the silicon thickness further reveals additional failure modes. Figure 2.4 shows SEM images for the case of 2.5 μm thickness, with other parameters the same as those in Figure 2.3. Here, bending induces some slipping, first observed at dL/L = 3.4 %, (R_{nom} ~10.2 mm, ε_{nom} ~0.25 %), as shown in Figure 2.4a. As the applied strain (dL/L) increases to much higher values of 53.4 % (R_{nom} ~2.6 mm, ε_{nom} ~0.98 %), the silicon is observed to delaminate from the substrate, as shown in Figure 2.4b. This third failure mode is driven by interface normal stresses (σ), i.e., peeling stresses. At even larger Si thicknesses, this delamination is observed without slipping. Figure 2.5a–c presents results for 10 μm thickness, with other parameters the same as those in Figure 2.4, except that L = 11.7 mm. Delamination begins at dL/L = 2.6 % (R_{nom} ~11.6 mm, ε_{nom} ~0.22 %) as shown in Figure 2.5a. The delamination initiates at the edges of the ribbons, and then propagates to the center as the bending increases (Fig. 2.5b and c). Removing the bending forces relaxes the system back to its initial flat state, without the sort of buckling that can be observed when slipping occurs.

Many similar considerations apply, in a qualitative sense, to the case of inward bending, which leads to compressive, rather than tensile, strains and stresses near the silicon. Figure 2.6 shows SEM images for the cases of ribbons with 700 nm and 10 μm thicknesses, and other parameters the same as those in Figure 2.5 except that L = 11.8 mm, after inward bending beyond the failure mode and then relaxing. In the case of 700 nm thickness, evidence of slipping was observed on the adhesive layer after relaxing from inward bending corresponding to dL/L = 29.7% (R_{nom} ~3.45 mm, ε_{nom} ~0.73 %) as shown in Figure 2.6a. The inset of Figure 2.6a shows that no such marks of slipping could be observed while in the bent condition (dL/L = 29.7%), due to the direction of the

slipping in this case. In other words, marks of slipping are hidden beneath the silicon in this configuration. Figure 2.6b presents, in the same manner, results for ribbons with 10 μm thickness. The slipping marks were observed after relaxing from inward bending of dL/L = 19.5 % (R_{nom} ~4.25 mm, ε_{nom} ~0.59 %). Practical considerations in imaging make it difficult to determine whether the delamination mode is present in these cases. Theoretical considerations, described in chapter 3, can address this issue.

2.3 Length Effects of the Ribbons

In addition to thickness, the lengths of the ribbons influence the bending mechanics, although direct measurements are difficult due to limited resolution in imaging and the small slip distances associated with the onset of failure. This section introduces an importance of the length of inorganic materials on plastic substrate approached by electrical properties.

Figure 2.7, a and b, shows SEM images for the cases of ribbons with 700 nm other parameters the same as those in Figure 2.3 except that the length of the ribbons are 500 μm and 50 μm, respectively. Onset of the slipping were observed at dL/L = 33.6 % in the case of short ribbon, although the slipping of long ribbon begins at dL/L = 9.0 %. However, the Si ribbon with short length was slipped in short distance which can be limited by imaging resolution. For this reason, as illustrated in Figure 2.8, electrical data from Si ribbon p-n junction diodes was used to illustrate the importance of ribbon length. The diodes consist of small arrays of ribbons each with thicknesses of 290 nm, doped to high concentration of phosphorous (n-type, ~10^{19}/cm^3) on one side and low concentration of boron (p-type, 6.0~9.4x10^{14}/cm^3) on the other, as shown in optical images of Figure

2.8. The n-type region was defined by spin casting a phosphorus containing spin-on dopant (Filmtronic) and then performing rapid thermal annealing (RTA, 950 ^oC, 5 s) to induce diffusion of the dopant. The p-type region was provided by the pre-existing doping level of the SOI wafers obtained from the vendor. The ribbons are placed on a PET substrate (175 μm thick) with an epoxy coating (~1 μm thick), in a manner similar to that of the test structures described in the previous sections except that L = 12.0 mm. For electrical contacts, ends of the ribbons were patterned with Ti/Au (thickness = 5/70 nm) deposited by electron beam evaporation and patterned by liftoff through a photlithographically patterned layer of photoresist (AZ5214). This metal covered the end parts of the silicon, the end edges of the silicon and the adjacent plastic substrate. The current (μA/ribbons) – voltage responses of the diodes were determined by making electrical contact to the metal on the plastic substrate near the devices, beyond the ends of the silicon ribbons. In this manner, the behavior of the ribbons on plastic substrate, which is induced by bending, is not affected by the probe tip. Figure 2.8a presents the current–voltage response of a representative diode that uses long (500 μm) ribbons, evaluated at different degrees of bending. The legend shows the nominal bend radius (R_{nom}). With increasing applied strain dL/L (i.e., decreasing R_{nom}), the on-current increases slightly. At the onset of slipping (dL/L= 5.0 %; R_{nom}~8.56 mm; ε_{nom}~1.02 %), the diode completely ceases to operate, due to loss of electrical contact between the metal probing pads and the silicon associated with fracture of the metal at the silicon edge, as shown in the inset of Figure 2.8a. In contrast, for ribbons with lengths of 50 μm (comparable to those useful for real devices, for example), the electrical performance of diode is stable under much higher degrees of bending (i.e., up to dL/L ~16.0 %; R_{nom} ~4.78 mm; ε_{nom} ~1.83 %) than

that of the longer devices as shown in Figure 2.8b. Moreover, these short devices also show good behavior during mechanical cycling (up to 200 cycles, from the flat state to bending at dL/L= 16.0 %) as shown in Figure 2.8c.

2.4 Other Implementations of the Concepts

This section suggests additional simple design modifications can improve the behavior beyond that described above.

Figure 2.9 illustrates two methods, with comparison to an unoptimized system (Fig. 2.9a) after bending beyond the slipping failure mode. The unoptimized case corresponds to silicon ribbons with 290 nm thickness, 20 μm widths and 500 μm lengths on PET sheet (175 μm thick) with length L = 12.0 mm, coated with an epoxy layer (~1 μm thick). (To observe the slipping mode with an optical microscope, the epoxy layer was postbaked after printing the ribbons. In this manner, a slight indentation appears in the epoxy, which can be observed by optical microscopy.) Figure 2.9a shows an optical image of these silicon ribbons during bending of dL/L = 30.8 % (R_{nom} ~3.44 mm; ε_{nom} ~2.54 %) which is much larger than that needed to initiate the slipping failure mode. The inset of Figure 2.9a provides a magnified view of the slipping region. By adding a thin, mechanically tough encapsulating layer on top of the inorganic layers, it is possible to increase both shear strength, τ_c, and tensile strength, σ_c. Details for these strengths are explained in chapter 3. Figure 2.9b, which shows an optical image of the silicon ribbons during bending of dL/L = 35.8 % (R_{nom} ~3.19 mm; ε_{nom} ~2.74 %), illustrates an example of this strategy using a ~2.5 μm thick layer of epoxy spin cast on top of Si ribbons, with other features of the system the same as those in Figure 2.9a. The inset of Figure 2.9b

shows the current (μA/ribbons) – voltage (V) response of diodes covered by the encapsulation layer with other parameters the same as those in Figure 2.7a. The diode operates up to dL/L = 35.0 % (R_{nom} ~3.23 mm; ε_{nom} ~2.71 %), but ceases to operate at dL/L = 40.0 % (R_{nom} ~3.02 mm; ε_{nom} ~2.90 %), due to slipping induced fracture of the metal at the silicon edge. Neutral mechanical plane concepts that involve the addition of PET and epoxy on top of the Si/epoxy/PET substrate, can be used as a further optimization. Figure 2.9c illustrates this type of layout (i.e., PET/epoxy/Si/epoxy/PET) and an optical image of Si ribbons during bending of dL/L = 57.8 % (R_{nom} ~2.5 mm). The image shows that the Si ribbons are stable without any failure at dL/L values that substantially exceed those associated not only with the slipping mode but also with cracking in the corresponding system without the PET/epoxy overlayers. These data are consistent with the ability of neutral mechanical plane concepts to provide high resistance to bend induce failure. The inset of Figure 2.9c shows the current (μA/ribbons) – voltage (V) response of p-n junction diodes in neutral mechanical plane layouts with other parameters the same as those in Figure 2.7a. In this layout, the current still flows through the diode at much higher degree of bending (dL/L= 50.0 % and 56.0 %; R_{nom}~2.55 mm and R_{nom}~2.70 mm) compared to the unoptimized system.

2.5 References

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2.6 Figures

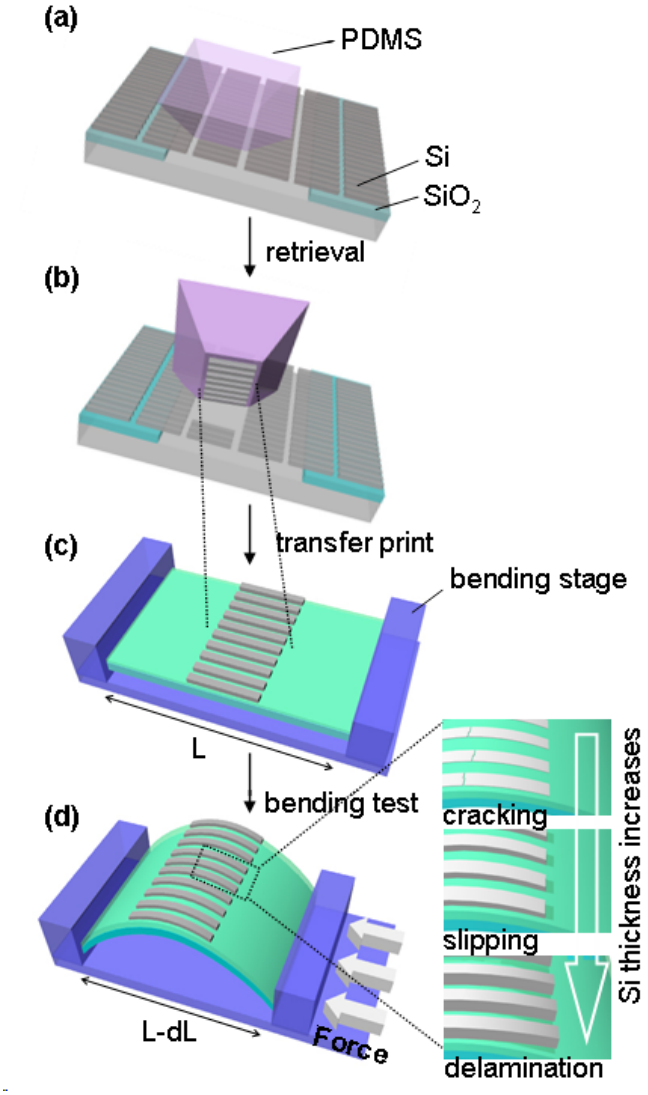

Figure 2.1 Schematic illustration of the steps (a)-(c) used to transfer-print Si ribbons from a silicon-on-insulator (SOI) wafer to a plastic substrate coated with adhesive layer and (d) the apparatus to evaluate the bending properties. At sufficiently large degrees of bending, various failure mechanisms (i.e. cracking, slipping, or delamination of the ribbons) can be observed, depending on the ribbon thickness, as shown on the right side of (d).

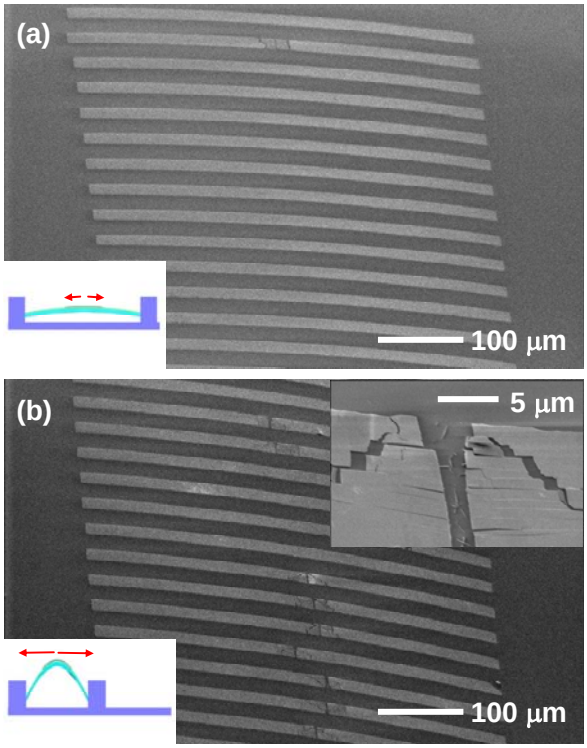

Figure 2.2 SEM images of bending in thin Si ribbons (thickness = 100 nm, width = 20 μm, length = 500 μm) on an epoxy(~1 μm)/PET (175 μm) substrate, corresponding to (a) dL/L = 35.6 % (R_{nom} ~3.15 mm, ε_{nom} ~2.78 %) and (b) dL/L = 45.8 % (R_{nom} ~2.78 mm, ε_{nom} ~3.15 %). The critical point for this cracking failure more is dL/L ~42.4 % (R_{nom} ~2.88 mm, ε_{nom} ~3.04 %). The bottom left insets provide schematic illustrations of the bending geometries. The inset of (b) shows a magnified view of the cracking.

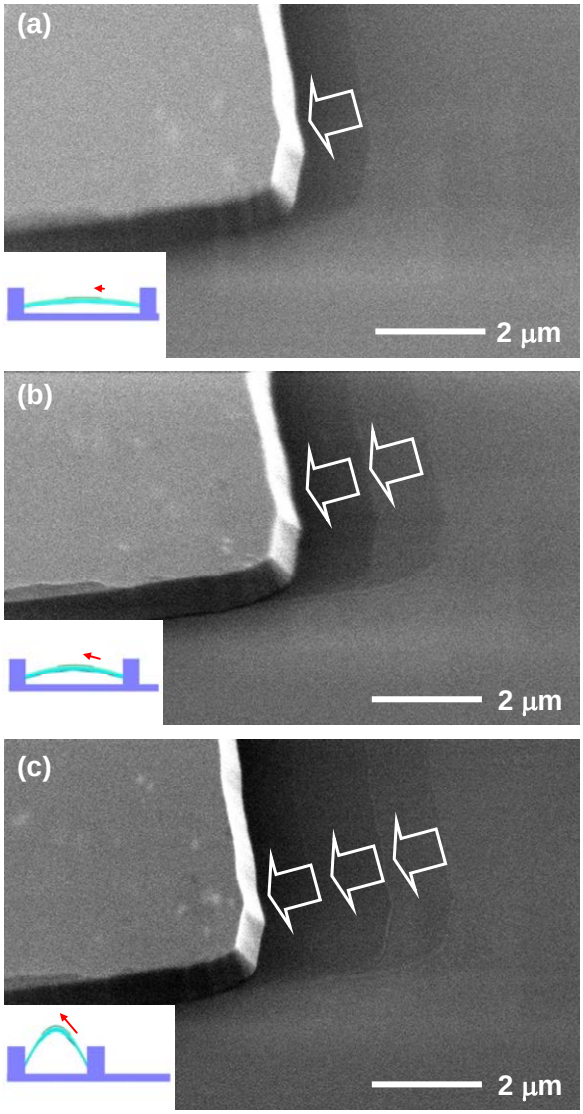

Figure 2.3 SEM images of bending in thin Si ribbons (thickness = 700 nm, width = 20 μm, length = 500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, corresponding to (a) dL/L = 9.0 % (R_{nom} ~6.26 mm, ε_{nom} ~0.40 %), (b) dL/L = 31.4 % (R_{nom} ~3.35 mm, ε_{nom} ~0.75 %) and (c) dL/L = 50.8 % (R_{nom} ~2.63 mm, ε_{nom} ~0.95 %). The bottom left insets provide schematic illustrations of the bending geometries. These images reveal of the progression of the slipping failure mode. Slipping begins at approximately dL/L ~9.0 %.

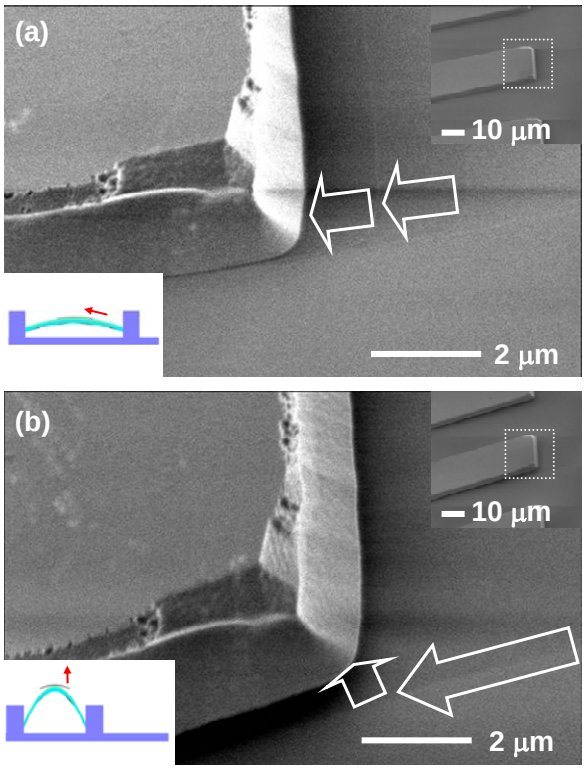

Figure 2.4 SEM images of bending in thin Si ribbons (thickness = 2.5 μm, width = 20 μm, length = 500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, corresponding to (a) dL/L = 3.4 % (R_{nom} ~10.2 mm, ε_{nom} ~0.25 %), (b) dL/L = 53.4 % (R_{nom} ~2.57 mm, ε_{nom} ~0.97 %). The bottom left and upper right insets provide schematic illustrations of the bending geometries and low magnification SEM images, respectively. These images reveal a failure mechanism that involves first slipping (a) followed by delamination (b).

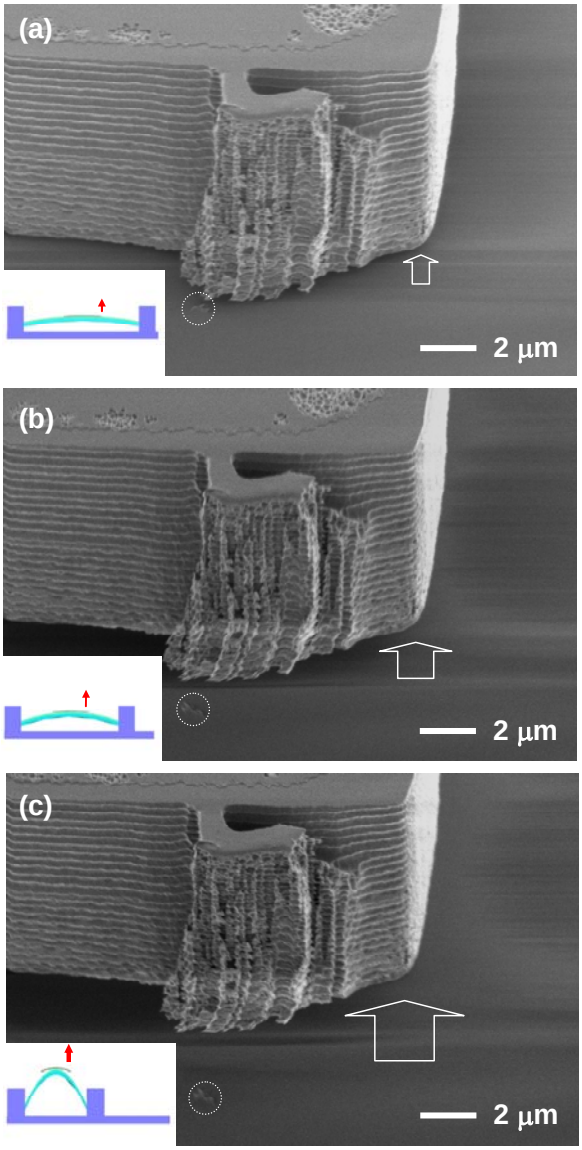

Figure 2.5 SEM images of bending in thin Si ribbons (thickness=10 μm, width=20 μm, length=500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, corresponding to (a) dL/L = 2.6 % (R_{nom} ~11.7 mm, ε_{nom} ~0.22 %), (b) dL/L = 4.3 % (R_{nom} ~9.06 mm, ε_{nom} ~0.28 %), and (c) dL/L = 6.0 % (R_{nom} ~7.67 mm, ε_{nom} ~0.33 %). The bottom left and upper right insets provide schematic illustrations of the bending geometries and low magnification SEM images, respectively. Delamination begins at about dL/L = 2.2 % (R_{nom} ~12.7 mm, ε_{nom} ~0.20 %) and increases with further bending. The fragment in white circle serves as a marker to track the movement of Si from the substrate. The bottom left insets provide schematic illustrations of the bending geometries.

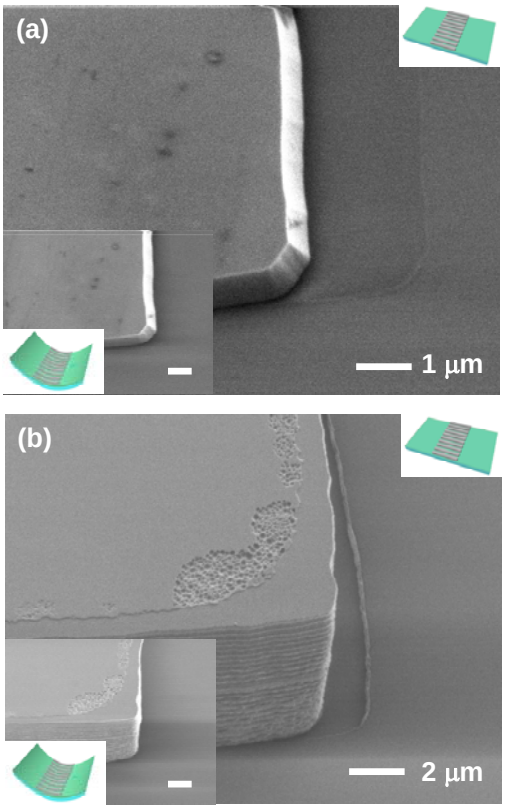

Figure 2.6 SEM images (a) of thin Si ribbons (thickness = 700 nm, width = 20 μm, length = 500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, collected in a flat state after inward bending to dL/L = 29.7 % (R_{nom} ~3.45 mm, ε_{nom} ~0.73 %) and (b) of thin Si ribbons (thickness = 10 μm, W/L = 20 μm/500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, collected in a flat state after inward bending to dL/L = 19.5 % (R_{nom} ~4.25 mm, ε_{nom} ~0.59 %). The upper right and lower left schematic illustrations show the configuration of the samples for the main frame and lower left inset SEM images, respectively.

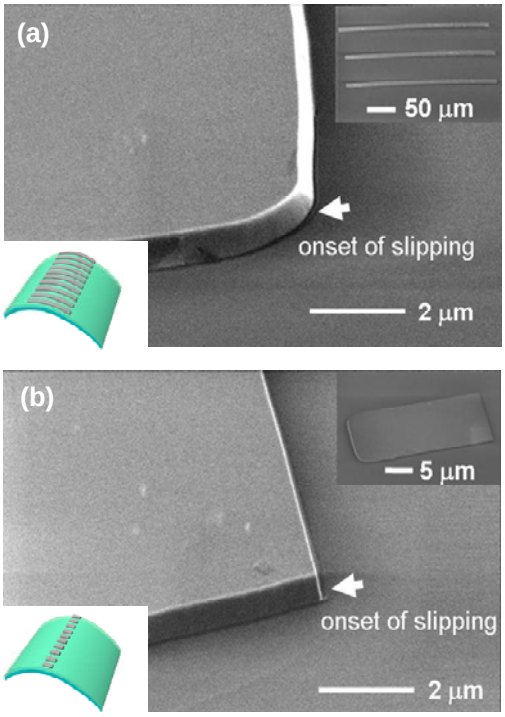

Figure 2.7 SEM images (a) of long Si ribbons (thickness = 700 nm, width = 20 μm, length = 500 μm) and (b) of short Si ribbons (thickness = 700 nm, width = 20 μm, length = 500 μm) on an epoxy(~1 μm)/PET (50 μm) substrate, corresponding to (a) dL/L = 9.0 % (R_{nom} ~6.26 mm, ε_{nom} ~0.40 %) and (b) dL/L = 33.6 % (R_{nom} ~3.24 mm, ε_{nom} ~0.77 %). The bottom left insets provide schematic illustrations of the bending geometries and low magnification SEM images, respectively. In case of (b), the Si ribbons slipped in short distance which can be close to imaging resolution.

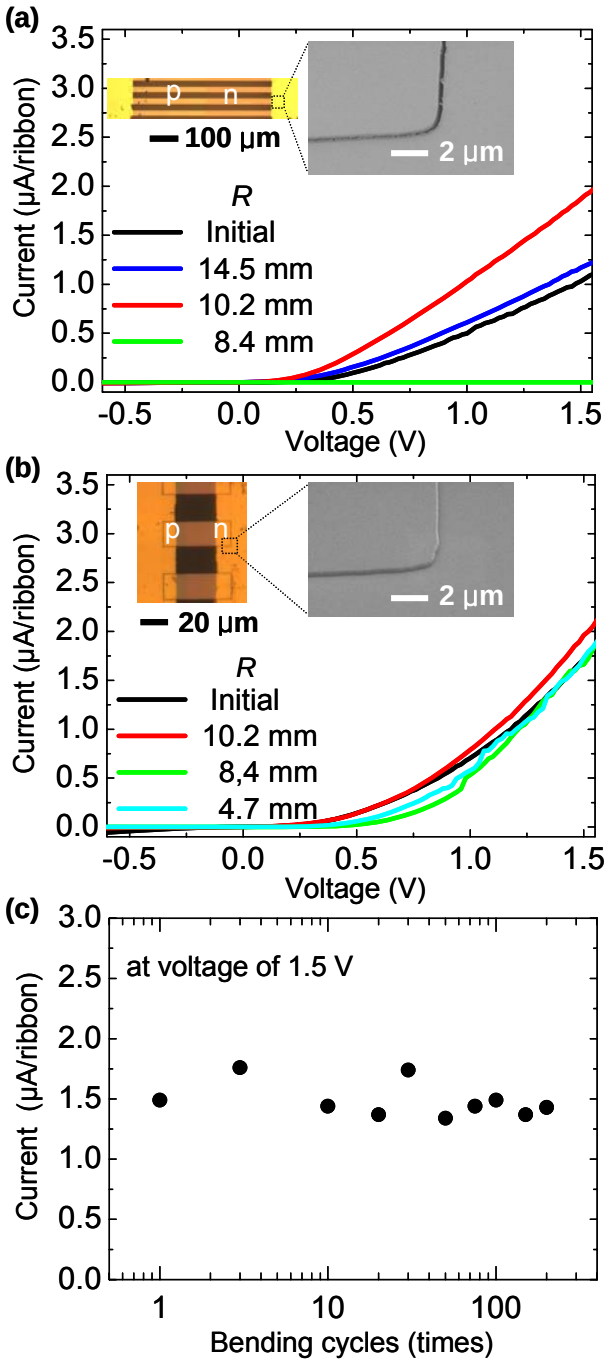

Figure 2.8 Electrical properties of diodes consisting of doped silicon ribbons with lengths of (a) 500 μm and (b) 50 μm under externally applied strain *dL/L*. The data correspond to current normalized to a single ribbon. (c) Current at 1.5 V and *dL/L* = 16.0 % as a function of bending cycles, i.e. after bending (to 16.0 % strain) and unbending devices several hundred times.

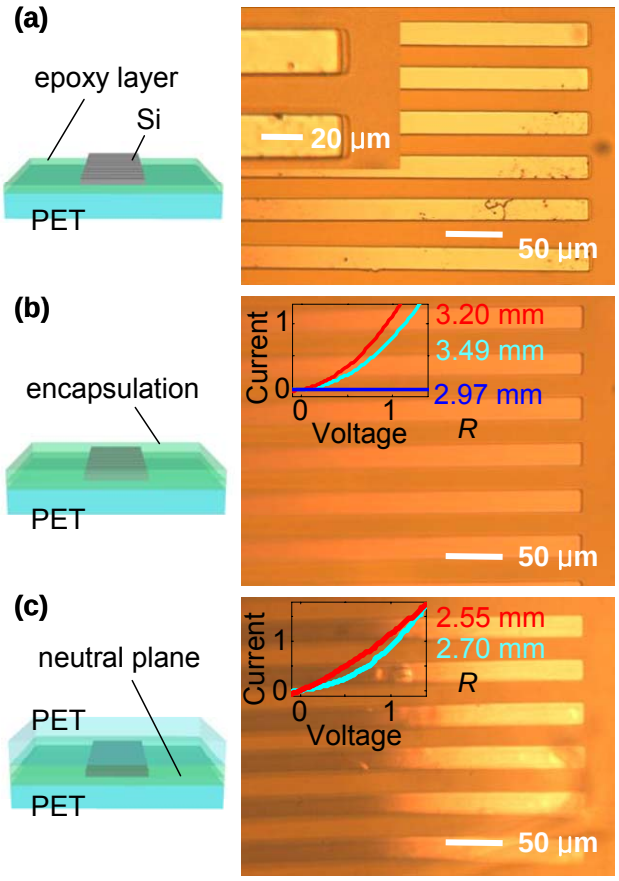

Figure 2.9 Optical images of (a) uncovered Si ribbons on the plastic substrate during bending (dL/L = 30.8 %, R_{nom} ~3.44 mm; ε_{nom} ~2.54 %) beyond the slipping failure mode, (b) encapsulated Si ribbons by epoxy with 2.5 μm thickness during bending (dL/L= 35.8 %, R_{nom} ~3.19 mm; ε_{nom}~2.74 %), and (c) Si ribbons on neutral mechanical plane made by PET and epoxy of the same thickness with bottom substrate during bending (dL/L = 57.8 %, R_{nom} ~2.51 mm). The substrate shown in these images is a 175 μm thick film of PET and an epoxy adhesive (~1 μm). The insets shows (a) optical image of a magnification of the slipping region and the current (μA/ribbons)-voltage (V) response of Si ribbon based simple p-n junction diodes with (b) encapsulation layer and (c) neutral mechanical plane layout.

CHAPTER 3: THEORETICAL STUDIES OF BENDING IN SINGLE CRYSTALLINE SILICON RIBBONS ON PLASTIC

This chapter discusses comprehensive theoretical studies of bending in structures relevant to inorganic flexible electronics based on the failure modes of the silicon (Si) ribbons on plastic, experimentally observed as described in previous chapter. Section 3.1 introduces simple, basic model to calculate the strain at the top surface of the device on the substrate in bending condition [1] and discussed a limitation of this model. Section 3.2 describes analytical mechanical models to understand different failure modes of inorganic materials on plastic substrate on bending as described in chapter 2. Section 3.3 discusses a length effect of inorganic materials on plastic substrate studied in chapter 2 using analytical modeling and finite element method. Section 3.4 addresses theoretical consideration relative to failure modes in inward bending described in chapter 2. Significant components of section 3.1 refer to a paper published in *Applied Physics Letters* in an article by Z. Suo *et al.* [1]. Significant components of section 3.2-3.4 were published as S.-I. Park, J.-H. Ahn, X. Feng, S. Wang, Y. Huang, and J. A. Rogers, "Theoretical and experimental studies of bending of inorganic electronic materials on plastic substrates," *Advanced Functional Materials* **2008**, *18*, 2673-2684 [2].

3.1 Simple Mechanical Models

This section presents simple mechanics models of film-on-foil devices on bending [1,3] and discusses its limitation to analyze accurate strain of inorganic materials on

plastic substrate and predict framework for understanding different failure modes on bending.

Figure 3.1 schematically illustrates simple film-on-foil structure on bending to understand strains at top and bottom surfaces and nominal plane (neutral mechanical plane) which has no strain [1, 3]. In flexible inorganic electronics, the strain at the top surface of the device substrate is approximated by [1, 3]

$$\varepsilon_{top} = \frac{h_f + h_s}{2R}, \tag{1}$$

where h_f, h_s, and R denote the film thickness, the substrate thickness, and the bend radius, respectively, with assumption of identical Young's modulus of film and substrate (Y_f=Y_s). In the case of the different Young's modulus ($Y_f \neq Y_s$), the strain at the top surface of the device substrate is given by [1,3]

$$\varepsilon_{top} = (\frac{h_s + h_f}{2R}) \frac{(1 + 2\eta + \chi\eta^2)}{(1+\eta)(1+\chi\eta)}, \tag{2}$$

where $\eta = h_f / h_s$ and $\chi = Y_f / Y_s$.

The devices placed in neutral mechanical plane enable to establish further bendibility in flexible inorganic electronics. If the stiffness of the device is negligible, the devices are placed in the neutral mechanical plane in the case of [1, 3]

$$Y_s h_s^2 = Y_e h_e^2, \tag{3}$$

where Y_e and h_e are Young's modulus and thickness of encapsulation layer, respectively. In this case, no strain is theoretically applied in the device in bending condition. In other words, the strain inducing failure of flexible inorganic electronic system is limited not by the device, but by the substrate and the encapsulation layer during the bending in this

case. Thin substrate with low Young's modulus and suitable encapsulation layer provide a route to achieve extremely small bending radii of curvature.

The degree of bendability is defined by the bend radius at which the strain reaches some substantial fraction of a fracture strain in a typical inorganic film (e.g., ~1%). However, the above calculations [1, 3] are still far too simple to provide either an accurate description of the mechanics or a predictive framework for understanding different modes of bending induced failure in these structures. Different from above mechanics models [1, 3], the analysis of bending strain in my doctoral research does not assume the thin film to cover the entire substrate, thereby explicitly accounting for effects of edges and finite device sizes, both of which play critically important roles in the mechanics and bending properties. These thin-film islands give non-uniform stress, with maxima that often appear at the edges and spatially non-uniform shear and normal stresses along the film substrate interface. These results are generally applicable to all classes of flexible inorganic electronics on plastic substrates. The observations and analysis explain all of the different failure mechanisms in unoptimized systems; they also rationalize the key mechanisms by which somewhat more advanced layouts can achieve enhanced robustness on bending.

3.2 Mechanical Models of Inorganic Materials on Plastic Substrate

Analytical mechanical models in this section provide in-depth understanding of different failure modes of inorganic materials on plastic substrate observed in bending condition as described in chapter 2.

The measurements were performed with the Si ribbons on plastic substrates with initial lengths L, subject to compression with external force applied through the bending stage. The experimentally measured L and L-dL can be used to compute the approximate, nominal bend radius (R_{nom}) defined near the center of the length of the substrate. This quantity is given by the reciprocal of the curvature of substrate as computed from the second derivative of the sinusoidal curve that describes the bent shape

$w = w_0 \sin\left(\pi X / L\right)$, where [4]

$$w_0 = \frac{2}{\pi} L \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12 L^2}} \tag{1}$$

and dL/L, h_s, w, and w_0 denote the applied strain, the substrate thickness, the deflection of the substrate in the z direction, and the deflection of the substrate at the center (i.e., $X=L/2$), respectively. This analysis applies to the experimental configuration, in which the ends of the substrate are free to rotate upon bending (i.e., they are unclamped). This bend radius, given by

$$R_{nom} = \frac{L}{2\pi \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12 L^2}}}\ , \tag{2}$$

is an approximate, global value that does not include the mechanical effects of the silicon. A corresponding, nominal bending strain, ε_{nom}, is defined as $h_s/(2R_{nom})$ [1, 3].

All of the observations described in chapter 2 can be understood using analytical models of the bending mechanics. To summarize these results, Table 3.1 presents the failure modes as a function of Si thickness (h_f). Thin Si ribbons (100 nm) on the 175 μm thick PET substrate exhibit the cracking mode, intermediate ribbons (290 nm ≤ h_f ≤ 1.25 μm) on the 50 μm thick PET substrate exhibit slipping (without any cracking) and thick

ribbons (10 μm) on the 50 μm thick PET substrate exhibit the delamination mode. Both slipping and delamination is observed, in sequence, with thicknesses in the range of 2.5 μm on a 50 μm thick PET substrate.

A modeling is based on beam theory in this section, as illustrated in Figure 3.2. This theory, as described below, can capture all of the key effects except the length dependence, which is discussed separately. The substrate is modeled as a beam of length L which is subjected to axial compression (Fig. 3.2a) to reduce the beam length to L-dL. Once dL/L reaches a critical strain $\pi^2 h_s^2 / 12L^2$ [4], the substrate bends, where h_s is the substrate thickness. For parameters characteristic of many of the experimental systems (i.e. L=11.8 mm and h_s=50 μm), this critical strain is 0.0015 %. As dL/L continues to increase, the axial compressive force (per unit width of the substrate) remains a constant [4]

$$F = \frac{\pi^2 E_s' h_s^3}{12L^2}, \tag{3}$$

where

$$E_s' = \frac{E_s}{1-\nu_s^2} \tag{4}$$

and E_s and ν_s are the Young's modulus and Poisson's ratio of the substrate. The bending moment in the beam is Fw, where the lateral displacement takes the form $w = w_0 \sin(\pi X / L)$, X = 0 and L denote two ends of the beam, and the maximum deflection w_0 is given by equation (1). This gives the nominal bend radius R_{nom} around the center as equation (2). The Si films are attached to the center of the top substrate surface via the epoxy adhesive layer (Fig. 3.2a). The film thickness h_f and adhesive layer

thickness h_a are much smaller than the substrate thickness, $h_f, h_a << h_s$, but the elastic modulus of silicon E'_f is much larger than its counterparts E'_s and E'_a of the PET substrate and epoxy adhesive layer, respectively, $E'_f >> E'_s, E'_a$. Therefore, the bending stiffness of the adhesive layer is much smaller than those of the films and substrate, $E'_a h_a << E'_f h_f, E'_s h_s$.

Figure 3.2b shows the system composed of a thin film, adhesive layer and substrate subjected to the axial compressive force F and bending moment $M = Fw_0$ (per unit width of the substrate). The film and substrate are modeled as beams, while a shear lag model is used for the adhesive layer due to its low stiffness. Jiang et al. (1997) and Wang et al. (2000) obtained the analytic solution for this problem [5,6]. The surface strain of the silicon film and the nominal bending strain ε_{nom}, defined by $h_s/(2R_{nom})$ [1,3], are shown versus the applied strain dL/L in Fig. 3.3a and b, respectively, for the 100 nm thick Si ribbons, 1 μm thick epoxy adhesive layer and 175 μm thick PET substrate. The surface strain of the film is much smaller than the nominal bending strain ε_{nom} because the adhesive layer relaxes the stretch transmitted from the substrate to the film.

The shear and peeling stresses along the film/adhesive interface reach a maximum at the tip (edge) of the film, and are responsible for the slip and delamination of interface, respectively. The maximum shear stress is given by [5,6]

$$\tau_{\max} = \frac{\pi G_a h_s}{\lambda h_a L} \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^2}{12 L^2}} \tag{5}$$

where G_a is the shear modulus of the adhesive layer and

$$\lambda = 2\sqrt{\frac{G_a}{h_a}\left(\frac{1}{E_f' h_f} + \frac{1}{E_s' h_s}\right)}. \tag{6}$$

The maximum peeling stress along the film/adhesive interface is given by [5,6]

$$\sigma_{\max} = \left[\beta G_a h_s \left(\frac{2\chi^3}{\lambda^2} + \frac{\lambda}{2} - \frac{\chi^2}{\lambda}\right) + E_a'\right] \frac{\pi}{\chi^2 h_a L} \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12L^2}}, \tag{7}$$

where

$$\chi = \left[3\frac{E_a'}{h_a}\left(\frac{1}{E_f' h_f^3} + \frac{1}{E_s' h_s^3}\right)\right]^{\frac{1}{4}}, \tag{8}$$

$$\beta = \frac{3\left(\frac{1}{E_f' h_f^2} - \frac{1}{E_s' h_s^2}\right)\frac{h_a}{G_a}\lambda}{4(1-\nu_a)\left(\frac{1}{E_f' h_f} + \frac{1}{E_s' h_s}\right)^2 + 6\left(\frac{1}{E_f' h_f^3} + \frac{1}{E_s' h_s^3}\right)\frac{h_a}{G_a}}, \tag{9}$$

and ν_a is the Poisson's ratio of the adhesive layer.

The maximum tensile stress in silicon films, which causes films to fracture, occurs at the center of the top surface, and is given by [5, 6]

$$\sigma_{crack} = \left\{G_a h_s \left[\beta\left(\frac{2\chi^4}{\lambda^3} + \frac{\lambda}{2}\right) - \frac{2h_f \chi^4}{3\lambda^2}\right] + E_a'\right\} \frac{3\pi}{\chi^4 h_f^2 h_a L} \sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12L^2}}. \tag{10}$$

In fact, the surface strain of the film shown in Figure 3.3 is given by σ_{crack} / E_f'.

The interface slip occurs when the maximum interfacial shear stress in equation (5) reaches the shear strength τ_c of the interface, i.e.,

$$\tau_{\max} = \tau_c. \tag{11}$$

For the 700 nm thick silicon film (and 1 μm thick epoxy adhesive layer and 50 μm thick PET substrate), the interfacial slip occurs at *dL*/*L*= 9.0 %. Equations (1), (5) and

(11) give the interfacial shear strength τ_c = 20.8 *MPa*, where the elastic properties of the film, adhesive layer and substrate are E_f= 130 *GPa*, ν_f= 0.27, E_a= 4.4 *GPa*, ν_a= 0.44, E_s= 4.0 *GPa* and ν_s= 0.44 [7,8]. Similarly, the interface delamination and film fracture occur when the maximum interfacial tensile (peeling) stress in equation (7) and tensile stress in the film in equation (10) reach the tensile strengths σ_c of the interface and σ_c^{Si} of the silicon film, respectively, i.e.,

$$\sigma_{\max} = \sigma_c \tag{12}$$

$$\sigma_{crack} = \sigma_c^{Si} \tag{13}$$

For the 10 μm thick silicon film (and 1 μm thick epoxy adhesive layer and 50 μm thick PET substrate), the interfacial delamination occurs at *dL*/*L*= 2.2 %. Equations (1), (7) and (12) give the interfacial tensile strength σ_c = 17.2 *MPa*. For the 100 nm thick silicon film (and 1 μm thick epoxy adhesive layer and 175 μm thick PET substrate), the silicon film fractures at *dL*/*L*= 42.4 %, and Eqs. (1), (10) and (13) give the strength of silicon film σ_c^{Si} = 1.0 *GPa*.

Figure 3.4 shows that the maximum interfacial shear and peeling stresses and film stress normalized by their corresponding strengths, $\tau_{\max} / \tau_c$, $\sigma_{\max} / \sigma_c$ and $\sigma_{crack} / \sigma_c^{Si}$, as a function of silicon film thickness, for 50 μm thick PET substrate. The thickness of the adhesive layer is 1 μm, and the applied strain is *dL*/*L* = 1.5 %. For each film thickness, the stress ratios $\tau_{\max} / \tau_c$, $\sigma_{\max} / \sigma_c$ and $\sigma_{crack} / \sigma_c^{Si}$ all increase with *dL*/*L*, and whichever reaches unity first causes the corresponding failure. Figure 3.4 suggests the film cracking and interfacial delamination for film thickness below 17 nm and above 6.2

μm, respectively, and interfacial slip for film thickness between 17 nm and 6.2 μm. This ribbon-thickness dependence of failure modes is consistent with experimental results in the prior chapter. It is important to point out that different failure modes depend on the film, adhesive layer and substrate properties, but not on the applied strain *dL/L* because all stress ratios are proportional to

$$\sqrt{\frac{dL}{L}-\frac{\pi^2 h_s^{\,2}}{12L^2}}\,.$$

Figure 3.5 shows the interfacial shear strength τ_c determined from the critical applied bending strain *dL*/*L* for interfacial slip measured from experiments at different film thickness. The interfacial shear strength is essentially independent of the film thickness, and is indeed a material property.

3.3 Mechanical Models of Length Effects

The analysis in section 3.2 is based on the beam theory, and therefore holds for the length L of silicon film much larger than the width W, for which the interfacial shear stress traction is mainly parallel to the ribbon direction. In most device configurations in electronics, the widths are comparable to the lengths, and therefore cannot be modeled as beams anymore since the interfacial shear stress tractions parallel and normal to the ribbon direction are on the same order. In this section, the finite element method was used to study the maximum interfacial shear stress, denoted by $\tau_{\max}^{plate}$. In here, the superscript "plate" is used to distinguish from the maximum interfacial shear stress in equation (5) from the beam theory, and the latter is now denoted by $\tau_{\max}^{beam}$. Figure 3.6a shows the three-dimensional (3D) model for the finite element analysis. The numerical results

suggest that the stress ratio $\tau_{\max}^{plate} / \tau_{\max}^{beam}$ is approximately a universal function that depends only on the ribbon length to width ratio, L/W, and is independent of material properties and thickness. The stress ratio $\tau_{\max}^{plate} / \tau_{\max}^{beam}$ is shown versus the ribbon length to width ratio L/W in Figure 3.6b, which can be well approximated by

$$\frac{\tau_{\max}^{plate}}{\tau_{\max}^{beam}} = 1 - \exp\left(-\frac{3\mathrm{L}}{4\mathrm{W}}\right). \tag{14}$$

This suggests that the ribbon length has essentially no effects (within 5% difference) for the ribbon length L four times larger than the width W. For $\mathrm{L} < 4\mathrm{W}$, the maximum interfacial shear stress decreases with the film length L, which agrees with the experiments reported in the previous section. This stress ratio decreases to about one half for the ribbon length equal to width, L=W. The combination of equations (11) and (14) gives

$$\tau_{\max}^{plate} = \frac{\pi h_s}{2L}\sqrt{\frac{G_a}{h_a\left(\frac{1}{E_f' h_f} + \frac{1}{E_s' h_s}\right)}}\sqrt{\frac{dL}{L} - \frac{\pi^2 h_s^{\,2}}{12L^2}}\left[1 - \exp\left(-\frac{3\mathrm{L}}{4\mathrm{W}}\right)\right]. \tag{15}$$

Figure 3.6b also shows the interfacial shear stress τ_{max}^{plate} versus the ribbon length to width ratio L/W. The applied strain *dL/L* (9.0%) is chosen such that the interface shear stress for long ribbons (thickness= 700 nm, width= 20 μm, length= 500 μm) on an epoxy (~1 μm)/PET (50 μm) substrate with length L = 11.8 mm just reaches the interfacial shear strength τ_c, which is marked by the dashed line in Figure 3.6b. For the same applied strain *dL/L*, the interfacial shear stress for short ribbons clearly falls short of the interfacial shear strength τ_c.

3.4 Analysis of Failure Modes in Inward Bending

The analysis in section 3.2 and 3.3 holds for outward bending illustrated in Figure 3.2a. This section addresses theoretical consideration relative to failure modes in inward bending described in chapter 2

For inward bending (buckling in the opposite direction), the bending moment changes the sign, $M = -Fw_0$. The interfacial shear stress also changes the sign, but its maximum remains the same as equation (5), and therefore gives the same τ_{max} / τ_c curve as Figure 3.4. The maximum interfacial peeling stress in equation (7) becomes compressive for inward bending. The interfacial peeling stress for inward bending reaches maximum at a distance away from the free edge, and the maximum is only a small fraction of equation (7) [5,6]. Therefore, the σ_{max} / σ_c curve in Figure 3.4 is much lower for inward bending, and consequently the interface slipping becomes the dominant failure mode. This is, in fact, consistent with our experiments which show interface slipping for both 700 nm and 10 μm thick Si ribbons on PET substrate.

3.5 References

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3.6 Table

adhesive layer	epoxy (1.0 μm)					
subs. thickness (μm)	175	50	50	50	50	50
Si thickness (nm)	100	290	700	1,250	2,500	10,000
fracture mode	crack	slipping	slipping	slipping	slipping+delamination	delamination
applied strain (dL/L, %)	42.4	23.7	9.0	5.9	3.4 / 53.4	2.6
nominal bend radius (mm)	2.88	3.86	6.26	7.73	10.2 / 2.57	11.6

Table 3.1 Critical applied strain of each failure modes as the Si ribbons thickness on plastic substrate coated with adhesive layer.

3.7 Figures

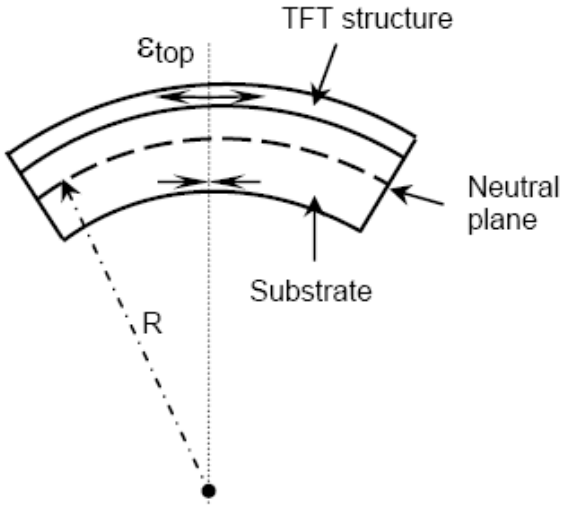

Figure 3.1 Schematic illustration of a film-on-foil structure on bending.

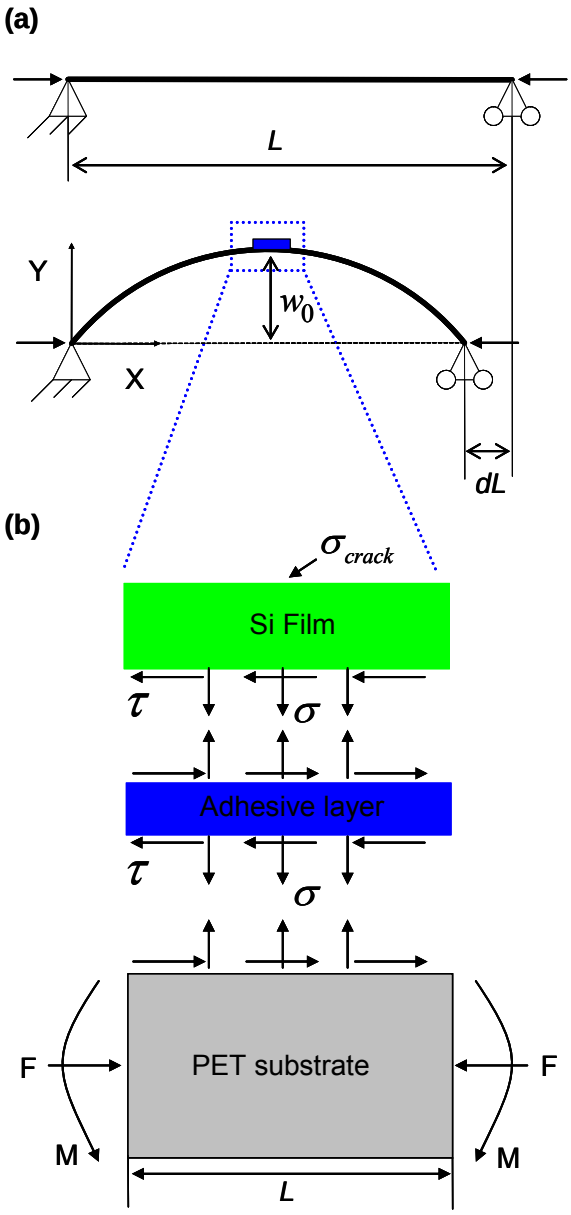

Figure 3.2 (a) Coordinate system of post-buckling analysis as a beam (b) stress analysis for a system composed of a thin film, adhesive layer, and substrate subjected to the axial compressive force F and bending moment $M = Fw_0$.

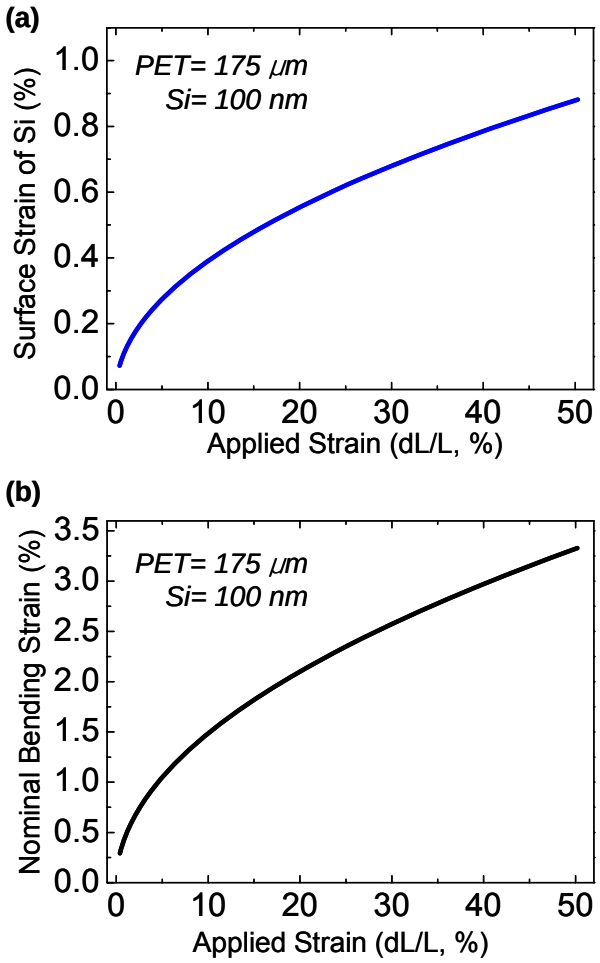

Figure 3.3 (a) Surface strain of silicon film; and b) nominal bending strain of PET substrate versus the applied strain dL/L for the 100 nm thick Si film, 1 μm thick epoxy adhesive layer and 175 μm thick PET substrate. The substrate a 175 μm thick film of PET and an epoxy adhesive (Si ribbons : thickness= 100 nm, W/L= 20/500 μm).

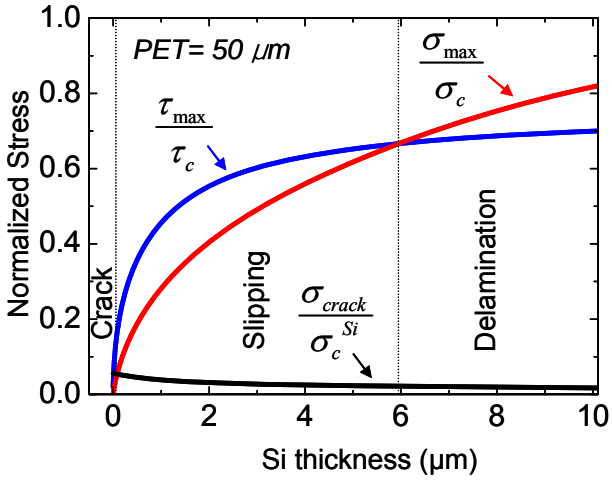

Figure 3.4 The stress to strength ratio versus the Si film thickness, which shows three failure mechanisms, namely the film cracking, interface slip, and interface delamination.

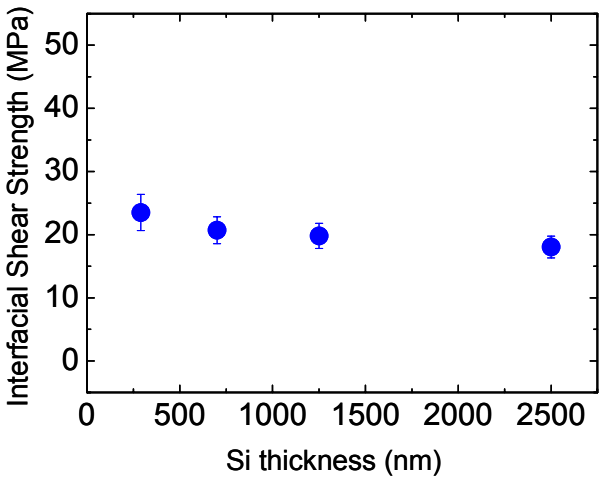

Figure 3.5 The interfacial shear strength determined from the slip of Si thin films with different thickness; the interfacial shear strength is essentially a constrant (τ_c = 20.7±2.2 MPa).

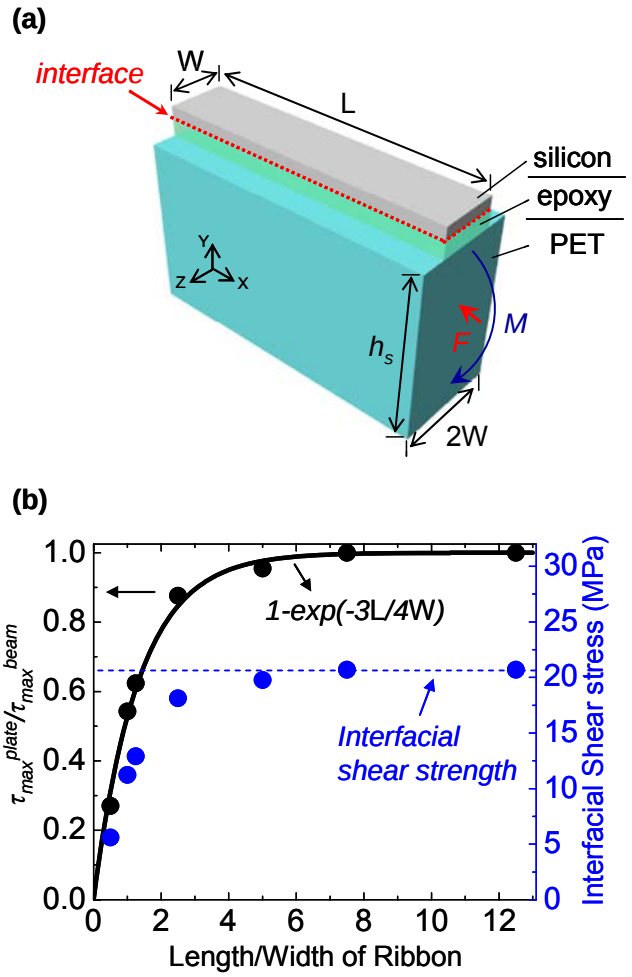

Figure 3.6 The length effect of Si ribbons on an epoxy(~1 μm)/PET (50 μm) substrate; (a) the model in the finite element analysis; (b) the maximum interfacial shear stress τ_{max}^{plate} obtained from the finite element analysis, and its ratio to the maximum shear stress τ_{max}^{beam} given by the beam theory, versus the ribbon length to width ratio, L/W.

CHAPTER 4: PRACTICAL APPROACHES IN SILICON PHOTOVOLTAICS

Chapter 4 and 5 present advanced approaches in practical applications based on the studies of behaviors of inorganic materials printed on plastic substrates on bending as described in chapter 2 and 3. This chapter reports highly bendable arrays of single crystalline silicon (Si) solar cells printed on plastic substrate. Section 4.1 describes a formation of ultrathin, single crystalline Si solar cells on conventional Si (111) wafer. Section 4.2 describes an approach to establish high bendability by use of array of solar cells described in section 4.1. Section 4.3 presents photovoltaic performance of this bendable array of solar cells and strain distributions in sheets of plastic substrates. Significant components of chapter 4 were published as J. Yoon, A. J. Baca, S.-I. Park, P. Elvikis, J. B. Geddes III, L. Li, R. Kim, J. Xiao, S. Wang, T.-H. Kim, M. J. Motala, B. Ahn, E. B. Duoss, J. A. Lewis, R. G. Nizzo, P. M. Ferreira, Y. Huang, A. Rockett, and John A. Rogers, "Ultrathin Silicon Solar Microcells for Semitransparent, Mechanically Flexible and Microconcentrator Module designs," *Nature Materials* **2008**, **7**, 907-915 [1] in a part of bendable array of ultrathin Si solar cells.

4.1 Fabrication of Ultrathin, Single Crystalline Silicon Solar Cell Arrays

This section describes the processing steps for fabricating ultrathin Si solar cells extracted from conventional single crystalline Si wafer (in here, Si (111)), which enable to be printed on foreign substrates such as a glass and plastic substrate.

Figure 4.1 schematically illustrates the processing steps for fabricating Si solar cells on bulk p-type Si (111) wafer (boron-doped, 10-20 Ωcm). The lateral dimensions of long ribbon type of Si solar cells (45 μm × 1.5 mm, width × length) are defined on p-type Si (111) wafer by reactive ion etching (RIE) through a patterned mask. The lengths of these structures are aligned perpendicular to the <110> direction of the wafer so that their long axes places along the preferential etching plane {110} for anisotropic, undercut etching with KOH, thus, which etches Si underneath Si (111) ribbons along the width direction of these structures. Regions of narrowed widths at the ends of the Si ribbons serve as anchors to retain their lithographically defined positions throughout the processing (homogeneous anchoring). Maintaining sharp-angled corners at the positions of these anchors leads to stress focusing for controlled fracture [1,2] in the printing step as shown in Figure 4.1 (upper right frame). After defining the lateral dimension of Si solar cells by RIE etching, selective-area diffusion of boron (p^+) and phosphorus (n^+) from solid doping sources through patterned diffusion barriers of SiO_2 creates rectifying p-n junctions and top contacts (Fig. 4.1, lower right frame). Deposition of etch masks (SiO_2/Si_3N_4, Cr/Au) on the top surfaces and sidewalls of the Si ribbons followed by KOH etching releases them from the source wafer everywhere except at the positions of the anchors (Fig. 4.1, lower left frame). Boron doping at the exposed bottom surfaces of the Si bars, again using a solid doping source, creates a back-surface field to yield fully functional Si solar cells. A cross sectional view of scanning electron micrograph (SEM) in Figure 4.1 provides a array of solar cells on a source wafer after undercut etching (in here, partially etched for easy view). These solar cells can be retrieved, by controlled fracture at the anchors, with an elastomeric polydimethylsiloxane (PDMS, Sylgard 184,

Dow Corning) stamp and then printed onto a target substrate, such as a glass, a plastic, or a rubber substrate, in a room-temperature process with overall yields of ~99.9% [3]. These solar cell designs and printing techniques described in this section enable new opportunities at the module level, with performance consistent with that of the individual cells. For example, the sequence in Figure 4.1 separates high temperature processing steps from the module substrate. As a result, integration of array of the solar cells on rollable, plastic sheets, for ease of transport and installation, is possible.

4.2 Fabrication of Highly Bendable Silicon Solar Cell Arrays

Based on this array of single crystalline silicon solar cells, highly bendable systems are demonstrated on plastic substrate. Figure 4.2 schematically illustrates the fabrication steps to establish this performance from a printed array of solar cells. Arrays of Si solar cells on the stamp press down into a liquid, photocurable polyurethane layer (NOA61, Norland Inc., ~30 μm) coated on the PET (~50 μm thick) as a handling substrate. The polyurethane layer takes roles as both an adhesive and planarization medium. The polyurethane fills the empty space between the Si solar cells by capillary action. Ultraviolet (UV) light exposures through the transparent PDMS stamp to cure the polyurethane layer and then removal of the stamp leaves the array of the solar cells on plastic substrate. The flat surface of the stamp coincides precisely with the top surfaces of the solar cells, to define the planarized surface of the module. Defining electrodes (Cr/Au, ~ 0.6 μm thick) by an etching process after metal evaporation completes the fabrication process. Optical image of Figure 4.2 shows a module that incorporates 130 solar cells on a glass substrate, where a photo-cured polyurethane (NOA61) serves as a planarizing

layer and as an adhesive for the printing process. This device was fabricated with a flat stamp to create a system with solar cells in arrangements that match those on the source wafer.

After transfer printing of array of solar cells on polyethylene terepthalate (PET; Grafix DURA-LAR, 50 μm thick) substrate coated with adhesive layer (NOA61), bendability was investigated. Unoptimized mechanical design causes a delamination of the Si ribbons from the substrate during the bending. Figure 4.3a-c shows the SEM images of single crystalline Si solar cells (50 μm × 1.5 mm, width × length, ~15 μm thick) on an polyurethane(~30 μm)/PET (50 μm) substrate, under bending along the length direction (dL/L= 0.0 %, 3.4 %, and 15.3 %). The Si ribbons are delaminated from polyurethane adhesive layer causing failure of interconnection with metal electrodes in a module level. The bendability of the Si ribbons was also investigated along the cell length and width directions in details as shown in Figure 4.4. The Si ribbons are delaminated from the adhesive at dL/L <3.5 % (R_{nom}>~9.8 mm) and dL/L ~7.6 % (R_{nom} ~6.8 mm) along the cell length and width directions, respectively. Electrical resistances support this failure mode induced a degradation of electrical property as shown in Figure 4.5. Figure 4.5, a and b, shows the SEM images at dL/L ~3.5 % (R_{nom} ~9.8 mm) and ~7.8% (R_{nom} ~6.7 mm) after a formation of metal interconnection (Fig. 4.2). The inset of Figure 4.5a shows initial state before the bending. White arrows in Figure 4.5a and b indicates the delamination of the Si ribbons from the adhesive (polyurethane). Figure 4.5, c and d, shows the SEM images of metal electrodes that generated cracks near the edges of the Si ribbons. As a result, this failure of the adhesion between the ribbons and the adhesive is propagated to the metal interconnection and causes the degradation of the

electrical performance. Figure 4.5e explains electrical resistances are abruptly increased as the applied strain is increased due to breaks of the metal interconnection.

High bendability can be achieved by optimized mechanical designs. As studied in chapter 1, the bendability of inorganic materials on plastic substrate can be improved by optimization of design, such as encapsulation, neutral mechanical design, and small dimension of inorganic materials on plastic. Due to lateral dimension of the Si solar cell (long length and short width), encapsulated structure was investigated in here. To optimize the thickness of encapsulation, a position of neutral mechanical plane and strain in bending along the cell length direction was modeled by a composite beam theory as shown in Figure 4.6, where W, W_{Si} and W_{NOA} are the widths of the beam, the Si cell and the distance between adjacent Si ribbons, respectively, and t, t_m, b and a-t are the thicknesses of the Si cell, metal interconnect layer, and polyurethane (NOA) layers above and below the Si cell. The Young's modulus of Si, metal (Au), and polyurethane are denoted by E_{Si} , E_{Au} and E_{NOA}, respectively. The parameters used in here are E_{Si} = 150 GPa, E_{NOA} = 1 GPa, E_{Au} = 78 GPa, a = 30 μm, t = 15 μm, t_m = 0.6 μm, W_{Si} = 50 μm, W_{NOA} = 26 μm. The strain in the beam is given by $\varepsilon_{yy} = (z - z_0)/R$, where R is the bending radius of the beam and z_0 is the position of the neutral mechanical plane. In this case (Fig. 5.6a), z_0 is given by

$$z_0 = \frac{a-t}{2}\frac{\left(1+\frac{b}{a-t}\right)^2 + 2\frac{b}{a-t}\frac{t+t_m}{a-t} + \frac{W_{NOA}}{W}\frac{t}{a-t}\left(2+\frac{t}{a-t}\right) + \frac{E_{Si}t}{E_{NOA}(a-t)}\frac{W_{Si}}{W}\left(2+\frac{t}{a-t}\right) + \frac{E_{Au}t_m}{E_{NOA}(a-t)}\left(2+\frac{2t+t_m}{a-t}\right)}{1+\frac{b}{a-t}+\frac{W_{NOA}}{W}\frac{t}{a-t}+\frac{E_{Si}t}{E_{NOA}(a-t)}\frac{W_{Si}}{W}+\frac{E_{Au}t_m}{E_{NOA}(a-t)}},$$

and is shown in Figure 5.6b. Analytical modeling indicates that this design with encapsulation layer (NOA61, ~30 μm thick) places the neutral mechanical plane near the

center of the solar cells are less than 0.3% even for bend radii less than 5 mm, for bending in any direction (that is, inward or outward, along the lengths of the cells or perpendicular to them). When neutral mechanical plane is placed in near middle of Si cell, Figure 4.6c shows the strain (ε_{yy}) at the top and bottom surface of Si cell with R = 4.9 mm using analytical expressions described above.

Finite-element modeling confirms these predictions in Figure 4.7. Figure 4.7a shows a composite structure consisting of a planarizing/adhesive layer (NOA61, ~30 μm), arrays of the Si solar cells and metal interconnects, and a polyurethane encapsulation layer (NOA61, ~30 μm) as described in processing steps of Figure 4.2. The finite element analysis is used to calculate the strain of the Si cell in bending along the cell width direction, as shown in Figure 4.7b, with R ~4.9 mm. The maximum strain in silicon for the inward and outward bending is around 0.03%. The maximum strain in the metal layer is around 0.13% and is located at the silicon corner for both inward and outward bending as shown in Figure 4.7b.

4.3 Performance of Bendable Array of Silicon Solar Cells

Performance of array of solar cells shows behavior consistent with expectation on the basis of mechanics analysis and relative insensitivity of the degree of illumination across the modest area of the module, for the bend radius examined here. The Bending was performed both directions (along the cell width and length directions) as shown in Figure 4.8a and b. Current (I) – voltage (V) characteristics was measured at bending radii of 12.6, 8.9, 6.3 and 4.9 mm, as shown in Figure 4.8c and d, along the cell width and length directions, respectively. The efficiency (~6.0 %) and fill factor (~0.60) remain

unchanged as summarized in Figure 4.8e. Fatigue tests were also performed by *I-V* characteristics along the cell width and length directions as shown in Figure 4.9a and b, respectively. Figure 4.9c shows the efficiency and fill factor do not have any noticeable change. The slightly reduced the efficiency and fill factor compared with the individual cell performance can be partially attributed to the shadowing effect and resistive losses arising from metal interconnects as shown in Figure 4.10.

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4.5 Figures

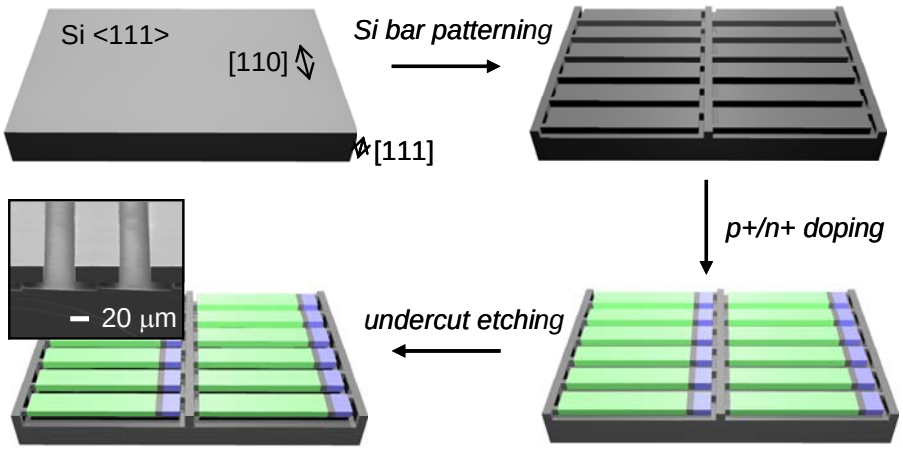

Figure 4.1 Schematic illustration of steps for fabricating ultrathin, single crystalline Si solar cells from a Si (111) wafer, which ready for transfer printing to a foreign substrate. SEM image shows cross sectional view of Si solar cell ribbons after partial undercut etching underneath Si ribbons.

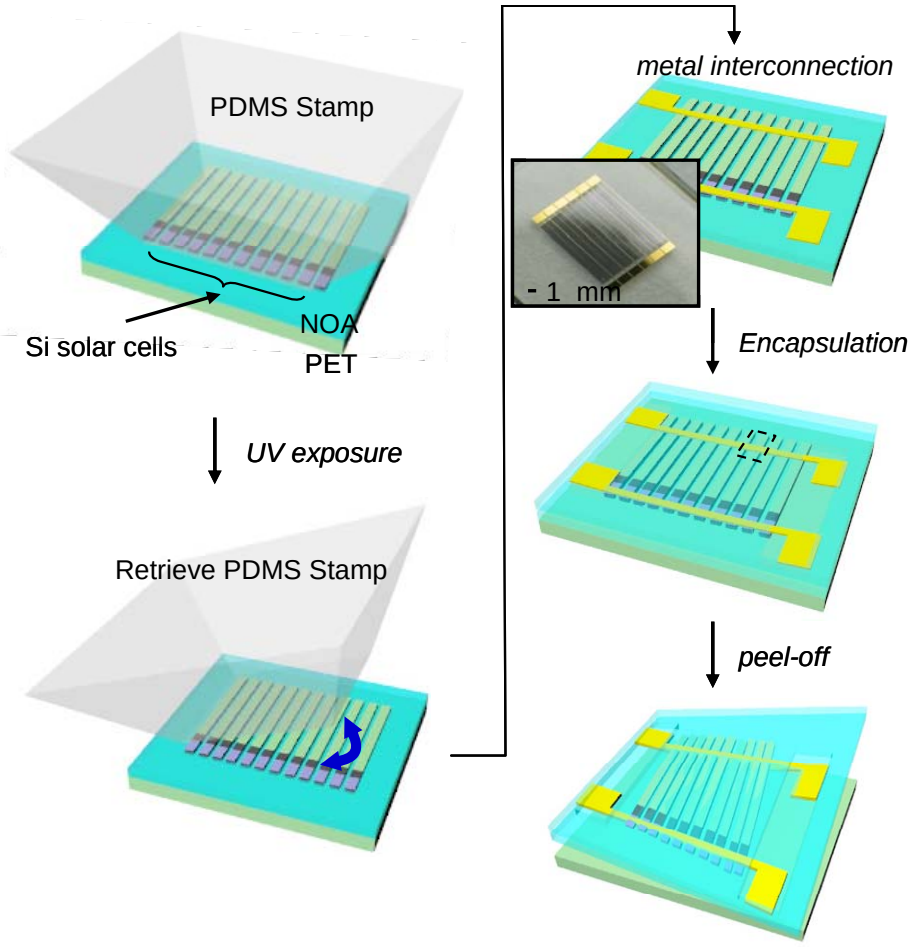

Figure 4.2 Schematic illustration of steps for printing ultrathin, single crystalline Si solar cells onto a plastic substrate and forming electrical interconnections to complete a module.

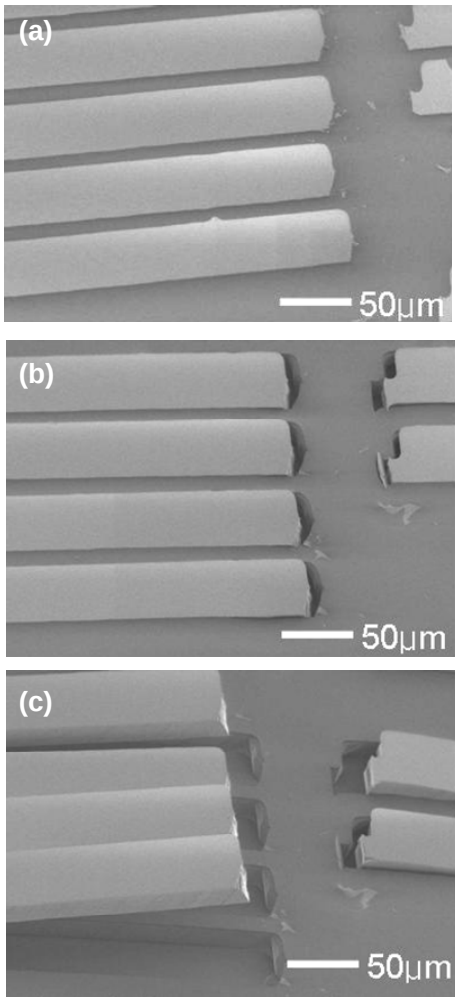

Figure 4.3 SEM images of bending in single crystalline Si solar cells (thickness=15 μm, width =50 μm, length=1.55 mm) on an polyurethane(~30 μm)/PET (50 μm) substrate, corresponding to (a) dL/L= 0.0 %, (b) dL/L= 3.4 % (R_{nom}~10.6 mm) and (c) dL/L= 15.3 % (R_{nom}~4.8 mm).

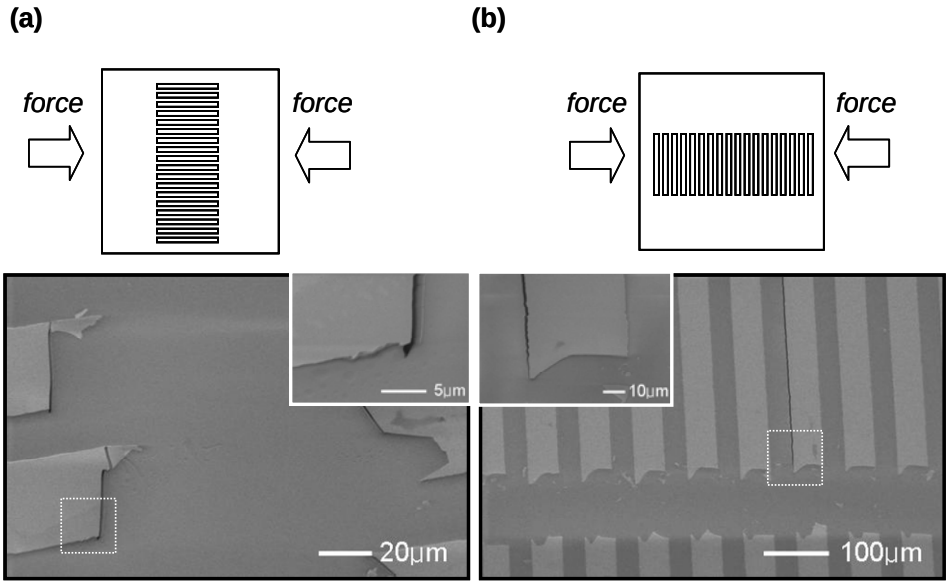

Figure 4.4 SEM images of single crystalline Si solar cells of bending along the cell (a) length and (b) width directions. Insets of (a) and (b) show SEM images of Si ribbons delaminated from the substrate coated with polyurethane layer at dL/L <3.5 % (R_{nom}>~9.8 mm) and dL/L ~7.6 % (R_{nom} ~6.8 mm), respectively.

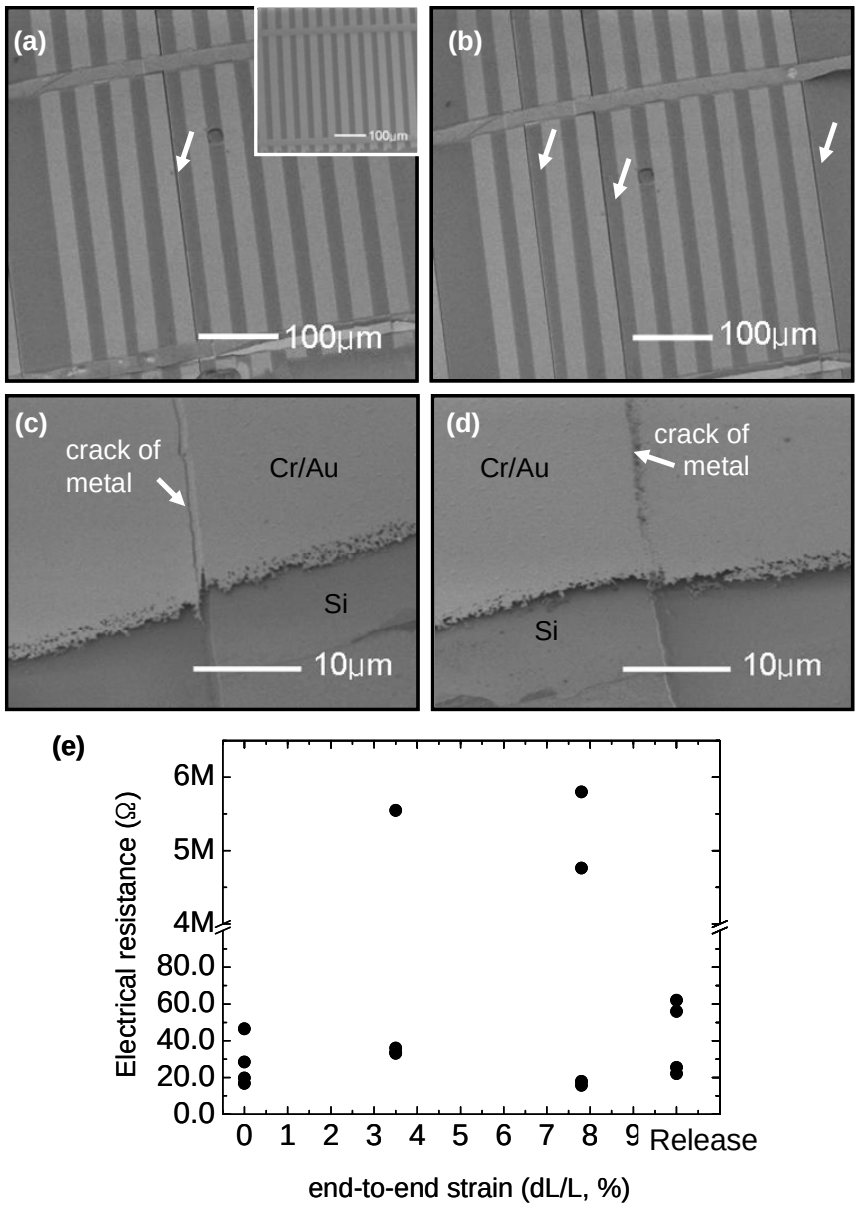

Figure 4.5 SEM images of single crystalline Si solar cells interconnected by Cr/Au electrodes on bending at *dL/L* (a) ~3.5 % (R_{nom} ~9.8 mm) and (b) ~7.8% (R_{nom} ~6.7 mm). The inset of (a) shows initial state before the bending. (c,d) SEM images of metal electrodes that generated cracks near the edges of the Si ribbons by the failure of the adhesion between the Si ribbons and the adhesive. (e) Electrical resistances of interconnected electrodes as a function of a bending strain.

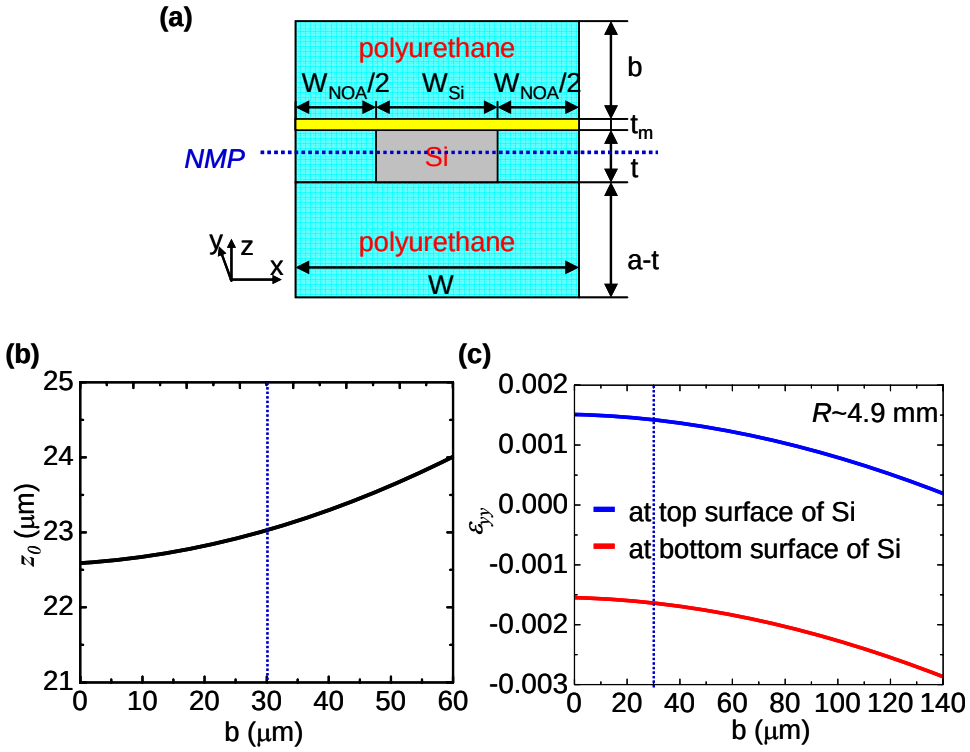

Figure 4.6 (a) Cross sectional schematic illustration of a model composite structure composed of Si cell, metal, and encapsulation layer, with key parameters. (b) Analytically calculated position (z_0) of neutral mechanical plane as a function of the top polymer thickness (b).

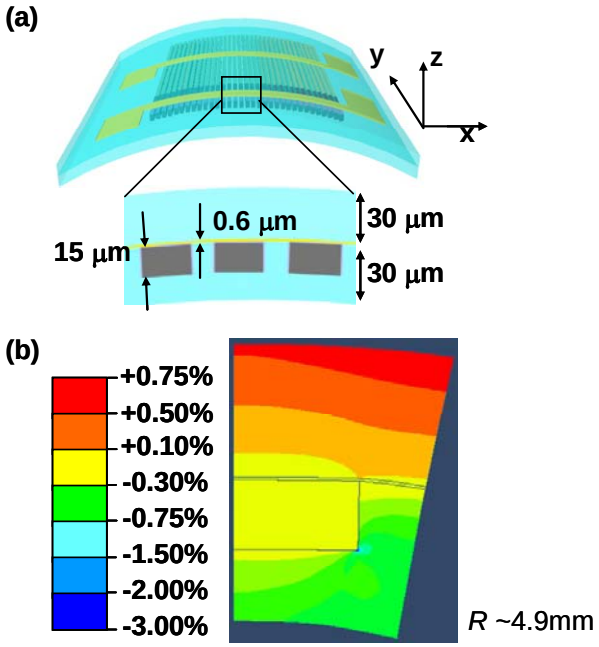

Figure 4.7 (a) Schematic illustration of an optimized design in which the neutral mechanical plane is positioned near the centre of the Si cells (gray) through judicious choices of thickness for the polymer (blue) substrate and overcoat. (b) Color contour plot of calculated bending strains (ε_{xx}) through the cross-section of a mechanically flexible Si cell module, bent along the cell width direction at R ~4.9 mm. The calculations use symmetry boundary conditions for evaluation of a single unit cell of the system. The black lines delineate the boundaries of the Si cell and metal interconnect line.

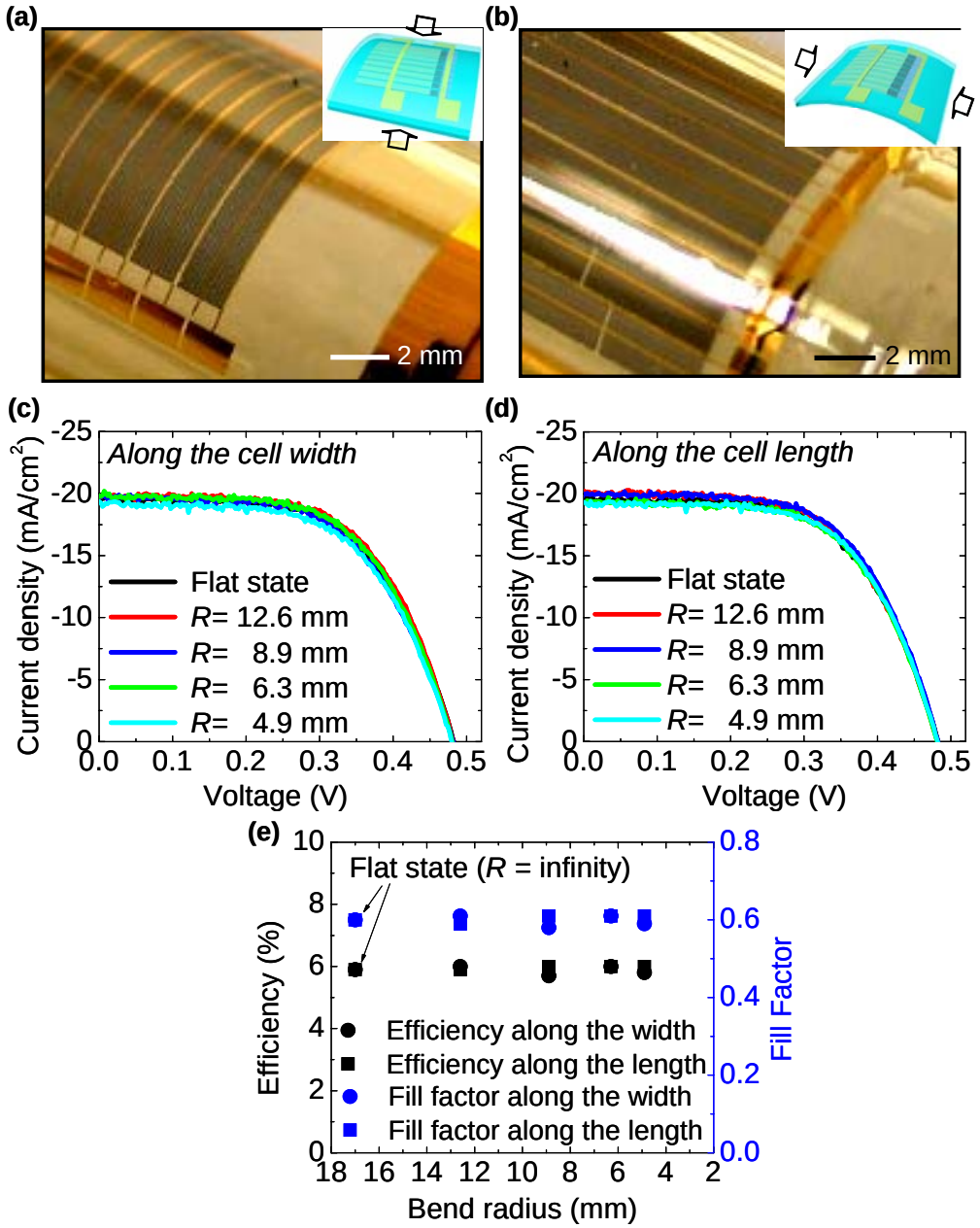

Figure 4.8 Optical imges of a mechanically flexible module based on the Si solar cells, bent along the cell (a) width and (b) length directions at R ~4.9 mm. Current density (J) – voltage (V) data from a mechanically flexible Si cell module under AM 1.5 illumination in a flat configuration and bent along the cell (c) width and (d) length directions, both for R = 12.6, 8.9, 6.3, and 4.9 mm. (e) Plot of the efficiency and fill factor under AM 1.5 illumination for R = 12.6, 8.9, 6.3, and 4.9 mm.

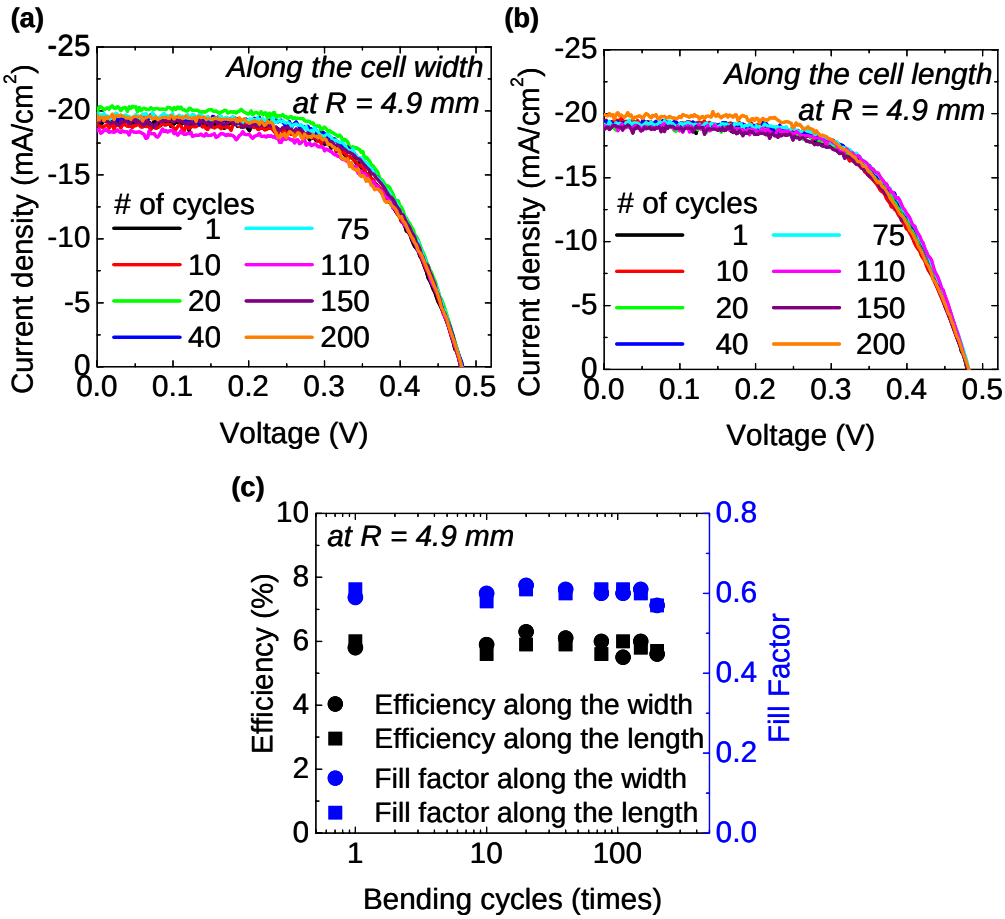

Figure 4.9 Current density (J) – voltage (V) data from a mechanically flexible Si cell module under AM 1.5 illumination in a flat configuration and bent along the cell (c) width and (d) length directions, both for R ~4.9 mm, during bending cycles up to 200 times. (c) Plot of efficiency and fill factor as a function of bending cycles up to 200 times at R_{nom} ~4.9 mm.

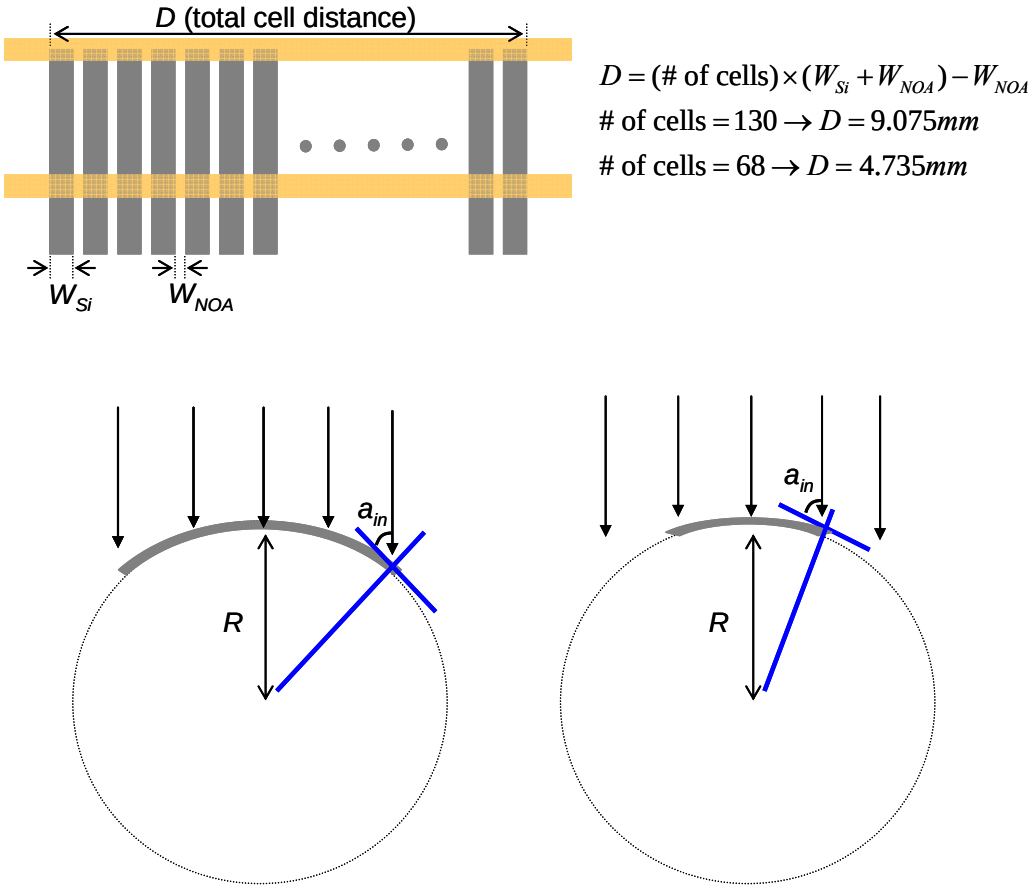

Figure 4.10 Schematic illustration of illumination geometry used for electrical characteristics of mechanically flexible Si solar cell module. The center of the module composed of 68 Si cells was aligned for normal incidence illumination, where the angle of incidence of light at the module edge is ~27° for R = 4.9 mm.

CHAPTER 5: PRACTICAL APPROACHES IN INORGANIC OPTOELECTRONIC SYSTEMS

This chapter presents printed III-V compound semiconductor inorganic optoelectronic systems, which have advanced flexibility, such as bendable, foldable, stretchable, and deformable properties, as important practical approaches about studies of behavior of inorganic materials on plastic substrates as mentioned in the previous chapters of this dissertation. Section 5.1 presents unpublished preliminary experiments to achieve high flexibility using prototype inorganic light-emitting diodes (ILEDs). Section 5.2 introduces epitaxial semiconductor multilayers design to yield ultrathin, microscale ILEDs and transfer printing techniques by polymer anchoring. Section 5.3 presents electrical connections of the small thickness (~2.5 μm) of the ILEDs enables the use of conventional thin-film processing. Section 5.4 and 5.5 describes strategies to establish flexible display, large area display with semitransparency, and stretchable lighting/display systems. Section 5.6 describes analytical modeling and simulation related to flexible and stretchable lighting/display systems. Section 5.7 describes analytical evaluation of mechanical strain sensitivity of emission wavelength in flexible and stretchable lighting/display systems. Section 5.8 reports advanced approaches designed to enable extremely high degrees of bendability and includes quantitative analysis of the underlying mechanics, with comparison to experimental measurements of bending induced shifts in the emission wavelength. Significant components of chapter 5 were published as S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K.-C. Hwang, P. Ferreira, X. Li, K. Choquette, and J.

A. Rogers, “Printed Assemblies of Ultrathin, Microscale Inorganic Light Emitting Diodes for Deformable and Semitransparent Displays,” *Science* **2009**, 325, 977-981 [1] except section 5.8. Significant components of section 5.8 is in press as S.-I. Park, A.-P. Le, J. Wu, Y. Huang, X. Li, and J. A. Rogers, “Light Emission Characteristics and Mechanics of Foldable Inorganic Light-Emitting Diodes,” *Advanced Materials* [2].

5.1 Flexible Inorganic Light-Emitting Diodes (ILEDs) Strip Lighting System

This section describes preliminary simple experiments using prototype inorganic light emitting diodes (ILEDs) for flexible inorganic lighting/display system on plastic substrates. This study in this section presents a potential possibility to achieve highly bendable optoelectronic system.

Figure 5.1 shows optical images of prototype ILEDs (RazerThin LEDs CxxxRT290-S0200, CREE Inc.) used in these preliminary experiments of flexible ILEDs strip lighting system on plastic substrate. A dimension of the ILED is 270 μm×270 μm×95 μm (width×length×thickness) and gold (Au) bond pads are placed on the top and bottom layers for a wire bonding. InGaN-based epitaxial multi layers generate an emission of blue light on SiC substrate (95 μm thick). In this study, conventional thin film processing was applied in a fabrication of the strip lighting system instead of the wire bonding in purpose of a reduction of total thickness of the lighting system. Figure 5.2a schematically illustrates processing steps for fabricating a simple one dimensional (1D) array of ILEDs strip lighting system. Thin polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning, ~10 μm thick) layer is formed on sheets of polyethylene terepthalate (PET; Grafix DURA-LAR, 175 μm thick). Metal electrodes (Ti/Au, 3 nm/100 nm) for

contacts with anode and cathode of the ILEDs are deposited by electron beam evaporation through a shadow mask. Individual ILEDs are manually picked and placed using fine tweezers on the bottom electrode on PET substrate coated with the PDMS, aligning with anodes of the ILEDs. In this way, the top electrode on PET substrate coated with the PDMS is placed on cathodes of array of the ILEDs. The optical micrograph of Figure 5.2a shows top and bottom electrodes are aligned with anode and cathode. The cross sectional view of Figure 5.2b schematically illustrates the placement of the ILEDs contacted to metal electrodes on top and bottom plastic substrates. Applying a voltage, the array of the ILEDs is emitted under bending (radius of curvature, R ~60 mm) as shown in an optical image of Figure. 5.2b. However, air gaps between those ILEDs causes a bad contacts with the electrodes so that the emission of the ILEDs is not reliable during repeated bending (R ~60 mm) and releasing cycles (Fig. 5.2c).

Figure 5.3 presents one of methods to achieve better bendability and reliability during repeated bending and releasing cycles. In contrast with the strip light (open structure) in Figure 5.2, the air gaps between the ILEDs are filled by an injection of adhesive materials (PDMS) in a vacuum state as shown in Figure 5.3a. Therefore, the ILEDs are surrounded by PDMS with no air gap except the metal contacts (filled structure). Figure 5.3b shows optical images of the strip light filled by the PDMS in operation at bending radii of ∞, 70, 50, and 30 mm, respectively. The emission from the ILEDs is improved during repeated bending (R ~50 mm) and releasing cycles (Fig. 5.3c). These results predict two structures (open and filled) provide different stress distributions near the ILEDs. Stress distributions are investigated by a finite element analysis as shown

in Figure 5.4a and b. The filled structure indicates the reduction of the stress at the electrode in the edge of the ILED compared to the open structure.

Total thickness and stiffness of the strip light are significant factors in bendability because an interface adhesion is relevant to a shear stress. Figure 5.4 demonstrates smaller radii of curvature can be achieved by simply applying thin substrates. The optical images of Figure 5.4, c, d, e, and f shows the strip light with the filled structure on thin sheets of polyimide (PI, 100 μm thick) wrapping on circular objects with bending radii of 30, 18, 12, and 8.5 mm, respectively.

In this section, the potential possibility was suggested to achieve flexible optoelectronic system, such as the filled structure and thin thickness of the substrate. However, the ILEDs used in this section have a thickness of ~95 μm, which is another significant factor given a limitation of bendability. However, most of thickness of the prototype ILED is from SiC substrate which is not for the emission, but for the epitaxial growth of InGaN-based ILED layers. Therefore, retrieval of the ILED from thick substrate enables to reduce total thickness of devices and improve the bendability.

5.2 Design and Transfer Printing of Ultrathin, Microscale ILEDs

This section presents epitaxial semiconductor multilayers designed for lateral delineation and release from a source wafer to yield isolated arrays of ultrathin, microscale ILEDs and transfer printing techniques for manipulating the resulting ILEDs in schemes that enable formation of large scale arrays on foreign substrates and in arbitrary spatial layouts.

Figure 5.5 shows the epitaxial semiconductor multilayers design for ILEDs, capable of release from a source wafer by undercut etching, grown on a GaAs wafer (Epiworks, Inc.). The epitaxial semiconductor layers include AlInGaP quantum well structures (6-nm-thick $In_{0.56}Ga_{0.44}P$ wells, with 6-nm-thick barriers of $Al_{0.25}Ga_{0.25}In_{0.5}P$ on top and bottom), cladding films (200-nm-thick layers of $In_{0.5}Al_{0.5}P$:Zn and $In_{0.5}Al_{0.5}P$:Si for the p and n sides, respectively), spreaders (800-nm-thick layers of $Al_{0.45}Ga_{0.55}As$:C and $Al_{0.45}Ga_{0.55}As$:Si for the p and n sides, respectively), and contacts (5-nm-thick layer of GaAs: C and 500-nm-thick layer of GaAs:Si for the p and n sides, respectively), for a total thickness of ~2.523 μm, all grown on AlAs (1500-nm-thick layer of $Al_{0.96}Ga_{0.04}As$:Si) on a GaAs substrate. The AlAs can be removed by etching with hydrofluoric (HF) acid, in procedures that do not alter the overlying layers or the underlying substrate. Figure 5.6 schematically illustrates the processing steps for releasing ILEDs from source wafer. The process for defining the ILEDs first involves forming a pattern of vertical trenches through the epitaxial layers by inductively coupled plasma reactive ion etching (ICP-RIE; Unaxis SLR 770 System, 2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W) through a mask of SiO_2 defined photolithographically (Fig. 5.6a, b). This step determines the lateral geometries of the devices. Creating a pattern of photoresist (PR) posts (i.e., “breakaway” anchors) located at two of the four corners of each island (Fig. 5.6c), followed by immersion in concentrated HF (Fig. 5.6d), leads to the undercut release of an organized array of ILEDs (Fig. 5.6e). Detailed processing steps are in Appendix A. The polymeric anchors hold the devices in their lithographically defined locations to prevent liftoff into the etching bath, even after complete undercut. Figure 5.7, a and b, shows top and cross-sectional scanning

electron microscope (SEM) images collected after this etching process for a representative case, where the device islands in Figure 5.7 are 50 μm × 50 μm. Next, an automated printing tool, as shown in Figure 5.8, brings a soft elastomeric stamp with features of relief embossed onto its surface into aligned contact with a selected set of these ILEDs. Peeling the stamp away fractures the PR anchors and leaves the devices adhered via Van der Waals interactions to the raised regions of relief. Figure 5.7, c and d, shows schematic illustrations of the printing process and an SEM image of an array of anchored ILEDs on the source wafer after one cycle of printing. The white arrows in Figure 5.7d highlight the collection of ILEDs removed by this process, corresponding to every third device along the two orthogonal axes of the square array. Figure 5.7e provides an SEM image of these devices printed onto a glass substrate coated with thin adhesive (PDMS, ~10 μm thick). Figure 5.9 shows schematic illustrations and optical micrographs of the printing process after three cycles using the ILED devices with 250 μm × 250 μm. The engineering design of the breakaway anchors is such that they are sufficiently robust to hold the ILEDs in their lithographically defined locations during the undercut etching and drying processes but sufficiently fragile to enable high-yield liftoff during printing. Detailed processing steps are included in Appendix A.

Three key design aspects are the use of (i) a pair of anchors on the same side of each ILED, to yield, after undercut, suspended, “diving board” layouts (Fig. 5.10a) that enable transfer of torques large enough to fracture the PR upon peel-back of the stamp; (ii) stamps with relief structures that are slightly smaller than the ILEDs and are offset from the centers of the devices to maximize these torques and also to minimize overlap with the anchors; and (iii) PR structures that fracture more readily than the semiconductor

material. This type of anchoring scheme (i.e., heterogeneous anchoring) is much more efficient in active materials utilization and versatile in design choices than corresponding methods demonstrated previously for transistors [3] and solar cells [4,5], where peripheral parts of the devices themselves serve as the anchors (i.e., homogeneous anchoring). Conventional wafer dicing and pick-and-place methods, as described in section 5.1, are not suitable for devices with the thicknesses and dimensions in the range reported in this section, due to challenges associated with wafer utilization, device fragility, and size. Such techniques also lack the high-throughput, parallel operation of the type of printing methods described above.

Figure 5.10b shows an optical image of a densely packed array of anchored, undercut ILEDs on a source wafer. Figure 5.10c shows sparse assemblies of these devices formed by printing in a step-and-repeat fashion from this wafer to a glass substrate, coated with a thin PDMS layer (~10 μm thick) to promote dry, conformal adhesion. Detailed processing steps are in Appendix A. As examples of high yields, large areas, and compatibility with plastic substrates, Figure 5.10d presents images of collections of ILEDs printed onto a thin sheet of PET (50 μm thick), shown as wrapped around a cylindrical glass support (1600 devices, in a square array with pitch of 1.4 mm; radius of cylinder ~25 mm) and onto a plate of glass (inset; 1600 devices, in a square array with pitch of 1.4 mm). The overall fabrication yields, including delineation and undercut of the ILEDs and subsequent printing of them onto the target substrates, were 100% in both cases. The devices were selected to have sizes (i.e., 250 μm × 250 μm) large enough to be visible in the images; those with sizes of Figure 5.7d are too small to be seen clearly at these scales.

5.3 Transfer Printing of Small ILEDs with 25umx25um Sizes

Establishing electrical connections to these printed ILEDs yields lighting elements or addressable displays. The small thickness (~2.5 μm) of the devices enables the use of conventional thin-film processing in comparison with the device (>~95 μm thick) in section 5.1, thereby providing a route to displays and related devices that is simpler, more scalable, and applicable to much smaller pixel geometries than established wire bonding and packaging techniques. This section presents electrical connections, by the use of conventional thin-film processing, to printed ILEDs to yield the emission and ohmic contact schemes, by low temperature annealing approaches, to improve electrical performance.

To demonstrate the most basic scheme, a collection of devices was transfer-printed onto a thin, metal mesh on a transparent substrate, to form bottom contacts, and then top contacts were separately established by the use of a planar lithographic process as shown in Figure 5.11. Detailed processing steps are in Appendix A. Figure 5.12 shows an exploded view schematic illustration and optical micrograph of an array of small, square devices (~25 μm × 25 μm), as well as those with shapes that spell "LED." following the processing steps in Figure 5.11. The results indicate bright emission, even out to the edges of the devices, consistent with the relatively low surface recombination velocity in AlInGaP materials [6, 7]. For improved performance, ohmic contacts can be implemented by using established metallization and annealing schemes [8, 9]. One strategy involves additional processing on the source wafer to yield released devices with integrated ohmic contacts, suitable for printing and interconnection even on low-

temperature substrates such as plastic or rubber. An alternative is to use low-temperature approaches to establish the ohmics directly on such substrates. For this work, the second strategy was studied, using processes that involve temperatures below 175°C. Figure 5.13 shows transmission-line model (TLM) analysis of the contact resistances associated with p contacts (Pt/Ti/Pt/Au = 10/40/10/70 nm) and n contacts (Pd/Ge/Au = 5/35/70 nm) to optimize annealing temperature and time necessary to low temperature processing on plastic substrate. Detailed processing steps are in Appendix A. Figure 5.14a shows the layout of an ILED with ohmic contacts printed onto a thin layer of polyurethane (NOA61, Norland Inc.) on a glass substrate, and an optical micrograph of emission from a directly probed device. Figure 5.14, b and c, presents electrical and optical characteristics of a set of such devices, recorded on the wafer before undercut etching and after printing. Emission spectra were measured using a spectrometer (Oceanoptics, HR4000) which enabled signal collected through an optical fiber directly mounted in an electrical probing station. The processing in this case used a passivation scheme to eliminate moderate degradation in performance associated with the HF etching step on unprotected devices as shown in Figure 5.15. The resulting current-voltage-emission behavior of the printed devices is comparable to that of the devices on the wafer.

5.4 Flexible ILEDs Display and Large Area ILEDs Display

This section describes promising routes to establish flexible display system and yield systems that cover areas much larger than those of the source wafer using inorganic LEDs and conventional thin-film processing as studied in section 5.3.

Figure 5.16 schematically illustrates processing steps of an interconnect scheme for passive matrix addressing. Photolithography and electron beam evaporation define patterned metal electrodes [Ti (20 nm)/Au (300 nm)] that connect p and n contacts (nonohmic for this case) of devices in common columns and rows, respectively. Two spin-cast, photopatterned layers of epoxy (~1.2 μm thick) provide openings to these contacts; the top layer electrically separates the column and row electrodes at their crossing points. Details are in Appendix A. Connecting terminal pads at the ends of these electrode lines to external computer control systems (Fig. 5.17) via ribbon cables that use anisotropic conductive films (ACFs) enables passive matrix addressing as shown in Figure 5.18. A small display in Figure 5.18 has 16 × 16 square array of ILEDs (50 μm × 50 μm) on a glass substrate with ACF ribbon cable connection.

Figure 5.19 and 5.20 show an exploded view schematic illustration of an interconnect scheme and optical images of flexible small display, wrapped around the thumb and wrist of a mannequin hand, that uses this design, formed on a thin sheet of plastic (PET, 50 μm thick) with a layer of a photocurable polyurethane (NOA61) as an adhesive. The ILEDs have dimensions of 100 μm × 100 μm and are configured into a 16 × 16 square array. The yields on the individual pixels for the case of Figure 5.19b and 5.20 are 100%; at the level of the display, one column and two rows do not function, due to breaks in the contacts to the ACF ribbon cable (Fig. 5.20a). Such systems can be bent to radii of curvature of ~7 mm, with no observable degradation, even for several hundred cycles of bending (Fig. 5.21). To evaluate the bending performance of flexible ILEDs displays, the displays were bent and released, with bend radii down to ~ 7.3 mm. The electrical properties of 32 different pixels in the display were measured and averaged to

assess the performance. To evaluate the fatigue performance of flexible ILED displays, multiple cycling tests were performed under repetitive bending and releasing up to 500 times (Fig. 5.21c, d). Electrical measurements were performed on 16 different pixels, for a bend radius of ~ 8.8 mm. Analytical calculation shows that even at the minimum bend radius investigated here, the maximum strain in the ILED is 0.21%, with a somewhat smaller strain (0.19%) in the quantum well region (see section 5.6 for details). Analysis using literature parameters to determine the dependence of the bandgap on strain [10–13] suggests changes in emission wavelength of ~2.4 nm for the smallest bend radius (see section 5.7 for details).

As shown in Figure 5.7 and 5.9, step-and-repeat printing can yield systems that cover areas much larger than those of the constituent ILEDs or the source wafer. One important outcome is the ability to form displays that can offer an effectively high level of transparency, where only the ILEDs (and the electrodes, if they are not made with transparent conductors) are opaque. Figure 5.22 shows examples of a 16 × 16 array, formed on glass. Here the area of the display is ~325 mm^2; the cumulative area of all the ILEDs is only ~2.5 mm^2, corresponding to less than ~1 % of the display area. Figure 5.22a illustrates the operation of such a system positioned above a sheet of paper with printed logos; the focus of the image is on the paper, thereby illustrating a practical level of transparency for application in a heads-up display, for example. Figure 5.22b shows the same device (lower left), operating in front of a mirror (upper right) to demonstrate bidirectional emission characteristics. The inset provides a magnified view of a region of this display, in its off state to show the small sizes of the ILEDs compared to the unit cells. These layouts are critically important for many applications, due to the efficient

utilization of the LED material, for reduced cost. For the examples shown, ~98% yields was achieved on the individual devices, and ~80% yields on the interconnections, limited by breaks in the metal lines and failed contacts to the ACF ribbon cable (Fig. 5.22c).

5.5 Stretchable ILEDs and Stretchable ILEDs Display

The devices and integration methods reported in this section are compatible with strategies to produce stretchable electronics [14, 15], thereby providing a route to conformable displays and lighting systems of the type that might be interesting for integration with the human body and other curvilinear, deformable surfaces, all of which demand more than simple bending (e.g., Fig. 5.19 and 5.20).

Figure 5.23a, as an example, schematically illustrates key processing steps for a stretchable ILED with the shape of a ribbon. This device was formed by transfer printing and bonding to a prestrained, rubber substrate of PDMS. Relaxing the prestrain creates a device with a "wavy," sinusoidal profile; this structure responds elastically to applied strain with a physics similar to that of an accordion bellows [14, 16] to yield a stretchable ILED device. Detailed processing steps are in Appendix A. Figure 5.23b shows optical micrographs of wavy ILEDs ribbons with 50 μm and 100 μm width collected with a scanning focal technique. Figure 5.23c-e show optical micrographs of a wavy ILEDs ribbon in different strained states from wavy to flat in the cases of non-emission with illumination, emission with illumination, and emission without illumination, respectively. I-V characteristics measured under different strained states as shown in Figure 5.23f. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

The wavelength and amplitude of stretchable ILEDs of Figure 5.23 were measured by a surface profiler (Sloan Dektak^3). A diamond stylus in contact with a sample surface scans along the length of ribbon and measures physical surface variation at different positions. In Figure 5.24, the top panels provide finite element simulation of the mechanics of the system in compressed (left) and stretched (right) configurations. The results indicate maximum strains in the ILED and the quantum well region of 0.36 % and 0.053%, respectively (see section 5.6 for details). The bottom panels show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively, in configurations similar to those illustrated in Figure 5.23. In more details, Figure 5.25 presents strain distributions in the devices, calculated by finite element analysis, of top surface, quantum well region, and bottom surface in a compressed state and quantum well region in a stretched state, respectively. The emission characteristics show no noticeable change in color with applied strain or associated changes in device geometry from "wavy" to flat (Fig. 5.26). This observation is consistent with a calculated change in emission wavelength of less than ~0.7 nm based on our computed strain values and analysis similar to that performed for the flexible display (see section 5.7 for details).

The "wavy" strategy of Figures 5.23-5.26 can accommodate only a relatively modest range of applied strains (i.e., up to a few percent, for the designs reported here). A path to displays with high levels of stretchability uses non-coplanar mesh designs adapted from schemes reported for integrated circuits [15]. Figure 5.27 presents key processing steps for fabricating 16 × 16 passive matrix, stretchable ILEDs display system. Here, interconnect lines between adjacent devices are supported by arc-shaped bridge structures

that can deform in response to applied strain. Details are in Appendix A. Figure 5.28a provides optical micrographs of four pixels in this display, in their off and on states, with (top) and without (bottom) external illumination, respectively, in compressed and stretched configurations. The images show the expected reduction in the heights of the arc-shaped bridges that lie in the direction of the applied tensile force (i.e., along the interconnects that run from lower left to upper right), together with an increase in the heights of the bridges in the orthogonal direction, due to the Poisson effect. This mechanical response is fully elastic—the bending-induced strains in the interconnects are small, the strains in the ILEDs are negligible, and the strain in the PDMS is well within its linear response regime. The data in Figure 5.28, b and c, are consistent with this mechanics, as are the associated mechanics calculations. In particular, the current (I) - voltage (V) characteristics of a typical device do not change in a measurable way for applied strains up to ~22%. No degradation of electrical property in I-V curves was observed on repeated stretching and compressing cycles. Stretching tests were performed with mechanical stages capable of applying uniaxial strain to evaluate the performance of stretchable ILED display under repetitive stretching and releasing up to 500 times (Fig. 5.28d). Electrical properties of 14 different pixels in the display were measured and averaged. In all cases, the testing was performed at a rate of roughly one cycle per second. Recent work demonstrates the use of smaller collections of large, conventional ILEDs in deformable devices that use different designs [17, 18]. Figure 5.29 and 5.30 present optical images of stretchable display, composed of a 16 × 16 square array of ILEDs bonded to a PDMS substrate and interconnected by electrodes supported by arc-shaped bridges, with a fraction of the pixels turned on (overall yield >80%). The shapes of these

bridges change in response to deformations of the display, in a way that isolates the ILEDs from any significant strains. In particular, calculation shows that for strains of 24 %, as defined by the change in separation between inner edges of adjacent device islands, the maximum strains in the ILED and quantum well are only 0.17 % and 0.026 %, respectively. The computed change in emission wavelength is less than ~0.3 nm (see section 5.6 and 5.7 for details).

5.6 Analytical Modeling and Simulation

5.6.1 Modeling of Flexible ILED Displays

The encapsulation, electrode, ILED, adhesive and plastic shown in Figure 5.16 can be modeled as a composite beam subject to a bend curvature. The distance between the neutral mechanical plane and the top surface in each cross section is given by

$$\sum_{i=1}^{N} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \Bigg/ \sum_{i=1}^{N} \bar{E}_i h_i \ , \qquad (1)$$

where N is the total number of layers, h_i is the thickness of the i^{th} layer (from the top), and $\bar{E}_i = E_i \big/ \left(1 - \nu_i^2\right)$ is related to the Young's modulus E_i and Poisson's ratio ν_i of the i^{th} layer. The strain in the ILED, including the quantum well, is given by y/R, where R is the bend radius, and y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for bendable display are (1) $E_{encapsulation}$ = 4.4 GPa, $\nu_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 4.0 μm and $h_{encapsulation2}$ = 0.877 μm for the two encapsulation layers above and below the electrode, respectively; (2) $E_{electrode}$ = 78 GPa, $\nu_{electrode}$ = 0.44, and $h_{electrode}$ = 300 nm; (3) E_{ILED} = 77.5 GPa, ν_{ILED} = 0.312, and h_{ILED} = 2.523 μm; (4) $E_{adhesive}$ = 1 GPa, $\nu_{adhesive}$ = 0.3, and $h_{adhesive}$ = 2.5 μm; and (5) $E_{plastic}$ = 4

GPa, $\nu_{plastic} = 0.44$ and $h_{plastic} = 50$ μm. These give the neutral mechanical plane 19.76 μm below the top surface. The maximum distance from the ILED is then 14.58 μm to the neutral mechanical plane, which gives the maximum strain 0.21% in the ILED for the bend radius $R = 7$ mm. The quantum well is 1.011 μm below the top surface of ILED (Fig. 5.5), and is therefore 13.57 μm to the neutral mechanical plane. This gives the maximum strain 0.19% for the bent radius $R = 7$ mm.

5.6.2 Modeling and Simulation of Stretchable ILEDs: the Wavy Design

As shown in Figrue 5.25, the stretchable ILED consists of the encapsulation, electrode and μ-ILED, and can be modeled as a composite beam with the effective tensile stiffness

$$\overline{EA} = \sum_{i=1}^{3} \bar{E}_i h_i \tag{2}$$

and bending stiffness

$$\overline{EI} = \sum_{i=1}^{3} \bar{E}_i h_i \left[\left(\sum_{j=1}^{i} h_j \right)^2 - \left(\sum_{j=1}^{i} h_j \right) h_i + \frac{h_i^2}{3} \right] - \frac{\left[\sum_{i=1}^{3} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \right]^2}{\overline{EA}} \tag{3}$$

where the summation is for the 3 layers of encapsulation, electrode and ILED, h_i is the thickness of the i^{th} layer (from the top), and $\bar{E}_i = E_i / \left(1 - \nu_i^2\right)$ is related to the Young's modulus E_i and Poisson's ratio ν_i of the i^{th} layer. The distance between the neutral mechanical plane and the top surface in each cross section is given by

$$\sum_{i=1}^{3} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \Big/ \overline{EA} \tag{4}$$

The device was formed by transfer printing and bonding to a pre-strained substrate of PDMS. Relaxing the pre-strain creates a device with a 'wave' of the amplitude *A* and wavelength λ. The bending energy and membrane energy of the wavy device are

$$U_{bending} = \frac{4\pi^4 \overline{EI} L A^2}{\lambda^4} \tag{5}$$

and

$$U_{membrane} = \frac{1}{2}\overline{EA}L\left[\pi^2\left(\frac{A}{\lambda}\right)^2 + \varepsilon_{pre}\right]^2 \quad , \tag{6}$$

where L is the length of device and ε_{pre} (<0) is the compressive strain on the device upon the release of the pre-strain in the PDMS.

The strain energy in the PDMS substrate due to the sinusoidal displacement profile on its top surface is

$$U_{substrate} = \bar{E}_s L \frac{\pi A^2}{4\lambda} \tag{7}$$

where $\bar{E}_s = E_s \big/ \left(1 - v_s^2\right)$ is related to the Young's modulus E_s and Poisson's ratio v_s of the PDMS substrate. The minimization of the total energy $U_{total} = U_{bending} + U_{membrance} + U_{substrate}$ gives analytically the wave length and amplitude as

$$\lambda = 2\pi\left(\frac{4\overline{EI}}{\bar{E}_s}\right)^{1/3} , \tag{8}$$

$$A = \frac{\lambda}{\pi}\sqrt{\left|\varepsilon_{pre}\right| - \varepsilon_{crit}} , \tag{9}$$

Where

$$\varepsilon_{crit} = \frac{3}{2}\left[\frac{\overline{EI}\overline{E}_s^{\,2}}{2\left(\overline{EA}\right)^3}\right]^{1/3} \tag{10}$$

is the critical strain for buckling.

The strain in the ILED, including the quantum well, is given by

$$4\pi^2 \frac{A}{\lambda^2} y, \tag{11}$$

where y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for the device are (1) $E_{encapsulation}$ = 4.4 GPa, $\nu_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 1 μm; (2) $E_{electrode}$ = 78 GPa, $\nu_{electrode}$ = 0.44, and $h_{electrode}$ = 10 nm; and (3) E_{ILED} = 77.5 GPa, ν_{ILED} = 0.312, and h_{ILED} = 2.523 μm. These give the neutral mechanical plane 2.22 μm below the top surface. The maximum distance from the ILED is then 1.31 μm from the neutral mechanical plane, which gives the maximum strain 0.36% in the ILED for the experimentally measured wavelength 275 μm and amplitude 5.15 μm. The quantum well is 1.011 μm below the top surface of ILED (Fig. 5.5), and is therefore 0.2 μm to the neutral mechanical plane, which gives a very small strain 0.053% in the quantum well.

The finite element method has also been used to determine the strains in the 1.0 μm-thick SU8 encapsulation, 10 nm-thick Au thin film and 2.523 μm-thick ILED on 1 mm-thick PDMS substrate. Eight-node, hexahedral brick elements (C3D8) and four-node multi-layer shell elements (S4R) in the finite element analysis software ABAQUS (2007) are used for the substrate and the thin film, respectively. The multi-layer shell is bonded to the substrate by sharing the nodes. Each layer of thin film is linear elastic, while the PDMS substrate is modeled as a hyper-elastic material. The eigenvalues and eigenmodes

of the system are first obtained. The eigenmodes are then used as initial small geometrical imperfections to trigger buckling of the system. The imperfections are always small enough to ensure that the solution is accurate. As shown in Figure 5.24 and 5.25, the numerical results give strains that agree very well with the analytical model.

5.6.3 Simulation of Stretchable ILED: the Island-Bridge Design

The finite element method has also been used to determine the strains in island-bridge design of stretchable ILED shown in Figure 5.27. Eight-node, hexahedral brick elements (C3D8) in the finite element analysis software ABAQUS (2007) are used for the substrate, which is modeled as a hyper-elastic material. Four-node, multi-layer shell elements (S4R) are used for the islands and bridges, which are linear elastic. The islands are bonded to the substrate by sharing the nodes, but the bridges do not. Figure 5.31 shows the strain distribution in the top, middle and bottom surfaces of the ILED as the bridge length is reduced from 310 μm to 250 μm. The maximum strain is 0.17%, and that in the quantum well is only 0.026%.

5.7 Analysis of Strain Sensitivity of Emission Wavelength

The calculated maximum uniaxial strains in the quantum well of the ILED system are 0.19% tensile in flexible ILED displays, 0.053% tensile in stretchable ILED, and 0.026% compressive in stretchable ILED displays. On the basis of the $k \cdot p$ perturbation theory [11, 12] for strain induced effect on semiconductor band structures, emission wavelength shift of the ILED associated with bending or stretching can be evaluated.

The bending and stretching deformations explored correspond to in-plane uniaxial stress defined as in the x direction here, and the stresses in the y and z directions are zero ($\sigma_{yy} = \sigma_{zz} = 0$) due to free contraction by Poisson's effect. Thus the strains in these directions are given by

$$\varepsilon_{yy} = \varepsilon_{zz} = -\nu\varepsilon_{xx} \quad (1)$$

where the Poisson's ratio ν is related to the elastic stiffness constants C_{11} and C_{12} by $\nu/(1-\nu) = C_{12}/C_{11}$. For the small stress range examined here, the strain induced bandgap shifts for heavy hole (HH) and light hole (LH) are given by $\delta Eg^{LH} = \delta E_H + \delta E_S$

$\delta Eg^{HH} = \delta E_H - \delta E_S$

where $\delta E_H = a\left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right)$, $\delta E_S = (b/2)\left(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}\right)$, and δE_H, and δE_S are the hydrostatic-pressure shift and the uniaxial stress-induced valence-band splitting, respectively [11-13], and a and b are the corresponding deformation potentials. For the quantum well ($In_{0.56}Ga_{0.44}P$) in the ILED structure, the parameters used for the present calculation are a = -7.42 eV, b = 1.91 eV, C_{11} = 11.936x10^{11} dyne/cm^2, and C_{12} = 5.975x10^{11} dyne/cm^2 [10]. Assuming HH is the ground state for the quantum well [10], the maximum uniaxial mechanical stress induced bandgap shift in the ILED system studied in previous section is calculated to be ~7.1 meV (or ~2.4 nm). This small shift can be considered negligible for most applications.

5.8 Light Emission Characteristics and Mechanics of Foldable ILEDs

This section reports advanced approach designed to enable extremely high degrees of bendability. The studies include quantitative analysis of the underlying

mechanics as described in section 5.6, with comparison to experimental measurements of bending induced shifts in the emission wavelength. The results provide strategies to achieve bending to radii as small as 0.7 mm with negligible changes in the electrical or optical properties of the devices. This outcome exceeds even the best levels of bendability in literature reports of OLEDs where bending radii as small as several millimeters have been achieved [19-22]. These outcomes might be useful for applications that require mechanical properties that are normally associated with OLEDs but with the performance achievable in ILEDs.

5.8.1 Experiments

Figure 5.32 schematically illustrates the key processing steps for fabricating the devices. Etching and release strategies first define microscale ILEDs from specialized epitaxial semiconductor layers grown on top of a sacrificial layer ($Al_{0.96}Ga_{0.04}As$) on a GaAs wafer (Fig. 5.5), following procedures reported in previous section. Techniques of transfer printing [1,2,14,23,24] lift these devices from the wafer and deliver them in sparse arrays onto sheets of PET (50 μm thick) coated with thin layers of a photocurable polyurethane (NOA61, spun at 5000 rpm/60 sec) as an adhesive. Next, wet etching through the top layers (p-GaAs /p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12), InAlGaP-based layers by HCl/H_2O (2:1), and n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12)) exposes just the n-GaAs at the base. In this way, contacts to the p and n sides of the device can be formed easily by planar, thin film processing of metal, as shown in Figure 5.32a. The SEM image of Figure 5.32a shows an angled view (45° tilted) of an individual ILED (width×length×thickness = 100 μm×100 μm×2.523 μm), partially embedded in the

polyurethane layer, after printing and etching. An epoxy coating (SU8-2, Microchem., spun at 1500 rpm/30 sec) prevents electrical shorting through the sidewalls of the ILEDs, and also provides partial planarization of the devices (total thickness ~2.5 μm) as illustrated in Figure 5.32b. Figure 5.32c shows electrodes used to establish electrical connection to the devices, formed by photolithography and etching of metallization (20/350 nm thick Ti/Au) deposited by electron beam evaporation. The optical micrograph of Figure 5.32c shows a top view. Figure 5.32d illustrates an encapsulation process that relies on epoxy material patterned to provide openings for electrical probing, and with different thicknesses in different regions. As described subsequently, the choice of thickness of the encapsulation layer is a key design parameter for controlling the bending mechanics. Multiple cycles of spin casting and photopatterning processes of epoxy layers (SU8-2, SU8-5) establish multiple thicknesses of encapsulation layer on the substrate. This layout leads to different strains in different ILEDs on a single substrate subjected to bending. The optical microscope image in Figure 5.32d shows emission from ILEDs with different encapsulation layer thicknesses (t_1 and t_2).

5.8.2 Light Emission Characteristics

Light emission of devices was characterized under bending by use of a high resolution spectrometer (Ocean Optics, HR-4000; ~0.5 nm resolution) and a multimode optical fiber (Thorlabs, 400 μm diameter core) as shown in Figure 5.33. The spectrometer has a resolution of ~0.5 nm, based on a HC-1 grating (200 ~ 1100 nm) and 5 μm slit width. The data points are reported in intervals of ~0.27 nm. Figure 5.33, a and b, shows a schematic illustration and an optical image of small, square lighting devices (100 μm ×

100 μm) formed on a thin sheet of plastic (PET, 50 μm thick) with a layer of a photocurable polyurethane (~2.5 μm) as an adhesive in a bending state, characterized by a radius of curvature, R, of ~7.3 mm. The optical fiber, as illustrated in Figure 5.33a, collects emitted light and transports it to the spectrometer. Figure 5.33c presents optical micrographs of individual ILEDs in operation at bending radii of ∞, 7.3, 4.9, and 3.5 mm, respectively. The optical images show that there is no observable change, even to the smallest bending radius (R ~3.5 mm). Current (I, log scale) – voltage (V) characteristics, as a function of bending radius of curvature, support these observations, as shown in Figure 5.33d.

On the other hand, the emission spectra show small, but systematic, changes with bending, as shown in Figure 5.34a for the case of an encapsulation layer with thickness of ~5.5 μm. In particular, as the bending radius decreases to R ~3.5 mm, the emission wavelength increases by ~3.8 nm±0.2 nm. These shifts were determined simply by recording the wavelength position of the peak in the emission spectra. These changes are attributable to shifts in the bandgap induced by mechanical strains. To explore this behavior in detail, the mechanics and the related bandgap shifts were analyzed as described in section 5.6 and 5.7. The system was treated as a composite beam. For the system of Figure 5.32d, the elastic properties and layer thicknesses are (1) $E_{encapsulation}$ = 4.4 GPa, $\nu_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 4.6 μm and $h_{encapsulation2}$ = 0.877 μm for the two encapsulation layers above and below the electrode, respectively; (2) $E_{electrode}$ = 78 GPa, $\nu_{electrode}$ = 0.44, and $h_{electrode}$ = 300 nm; (3) E_{ILED} = 77.5 GPa, ν_{ILED} = 0.312, and h_{ILED} = 2.523 μm; (4) $E_{adhesive}$ = 1 GPa, $\nu_{adhesive}$ = 0.3, and $h_{adhesive}$ = 2.5 μm; and (5) $E_{plastic}$ = 4 GPa, $\nu_{plastic}$ = 0.44 and $h_{plastic}$ = 50 μm. The neutral mechanical plane is 20.2 μm below

the top surface. The maximum distance from the quantum well to the neutral mechanical plane is then 13.4 μm, which gives a maximum strain of nearly 0.4 % in the quantum well for a bending radius R = 3.5 mm. The expected strain dependence of the emission wavelength can be evaluated with $k \cdot p$ perturbation theory as described in section 5.7 [1,11-13]. The uniaxial mechanical stress induced bandgap shift in the ILED is ~4.9 nm, for a maximum bending strain of ε_{xx}=0.384 %.

Figure 5.34b shows the calculated emission wavelength shift (black) and experimentally measured shifts (various colors; error bars comparable to symbol sizes) as a function of the calculated maximum uniaxial strain in the quantum well of the ILED. The strains depend both on the bending radii (7.3 mm, 4.9 mm, and 3.5 mm) and the thickness of the encapsulation layer. The calculations show reasonably good agreement with measurement, thereby providing some validation of the underlying physics. Many similar considerations apply to inward bending, which leads to compressive strains in the quantum well. Figure 5.34c shows the emission spectra in cases of both inward and outward bending. Outward bending leads to increases in the wavelength (red shift, $\Delta\lambda$ ~1.77 nm) at a bending radius of 4.9 mm. By contrast, inward bending (R ~5.4 mm) reduces the wavelength (blue shift, $\Delta\lambda$ ~-1.27 nm). The calculated maximum strains in the quantum well of the ILED system in these two cases are 0.275 % tensile and 0.250 % compressive. Slight discrepancies between experiment and theory can be caused by compositional variations, defects induced by compressive strains during fabrication, or uncertainties in values of parameters (moduli, dimensions or electronic properties) used in the modeling.

5.8.3 Foldable ILEDs

Although the magnitudes of the shifts in emission wavelength for the examples shown previously are likely to be unimportant for most applications, strategies that reduce the strains that give rise to these shifts can minimize mechanically induced degradation at interfaces or, ultimately, fracture in the devices. One solution is to configure the layouts to place the ILEDs near the neutral mechanical plane. The position of this plane can be computed by equation (1) in section 5.6.

Figure 5.35a shows a schematic illustration of a layout that achieves this outcome. A photocurable polyurethane (NOA61) is spin-coated (3000 rpm/60 sec), cured by UV exposure for 1 hour on a temporary substrate of PET. The fabrication of ILED devices follows the processing steps described in section 5.8.1. Except for metal probing, the devices formed in this way are encapsulated by the polyurethane and lie near the mechanical neutral plane after removing the PET. The total thickness of sheet is ~17 μm which includes the ILEDs, the epoxy interlayer, the metal electrodes and the polyurethane layers. In this configuration, the system can be bent to sharp folds, with R as small as 0.7 mm, with associated wavelength shifts of ~1 nm, close to the resolution limit of our spectrometer (~0.5 nm) and simple means for evaluating the shifts as shown in Figure 5.35b. Figure 5.35c describes the calculated maximum strain in the quantum well of the ILED for the previously described encapsulated scheme on PET and the neutral mechanical plane design as a function of bending radius. The labels a, b, c, and d correspond to PET, polyurethane, epoxy, and ILED, respectively, in the schematic cross sectional views that appear as insets in Figure 5.35c. The maximum strain in the quantum well of the ILED decreases as the top encapsulation layer is increases for the devices on

PET. In nearly neutral mechanical plane designs, the maximum strain in the quantum well dramatically decreases as top polyurethane and epoxy layers match the mechanical effects of the bottom polyurethane layer. Figure 5.35d shows the dependence of the shift in emission wavelength on the bending strain as a function of the encapsulating layer thickness. The shifts dramatically decrease as the ILED moves toward the neutral mechanical plane. This design provides extreme levels of bendability, as shown in Figure 5.36a for the case of an ILED (100x100 μm) wrapped around the edge of a slide glass (thickness ~1 mm), respectively. The left frame in Figure 5.36b shows a cross sectional optical micrograph; the bending radius is approximately 0.7 mm. For this case, relatively large size ILEDs (500x500 μm) were used, for ease of viewing. The curved lines (red) indicate of the approximate locations of the devices. The right frame in Figure 5.36b shows a composite optical image, formed using images captured at different focal depths, of a 3x3 square array of ILEDs. Figure 5.36c provides a slightly different view of a similar array. In both images, bending of the ILEDs themselves can be clearly observed.

5.9 References

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5.10 Figures

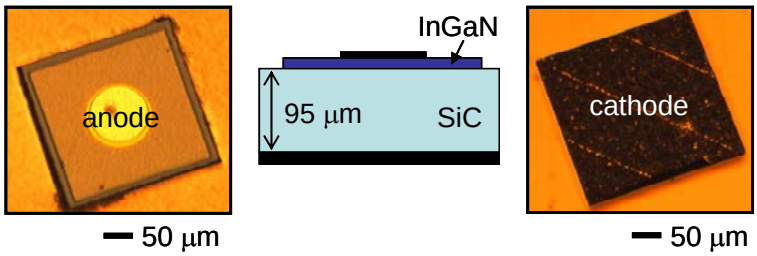


Figure 5.1 Optical micrographs of top (left) and bottom (right) sides and cross sectional geometry of prototype ILED (RazerThin LEDs CxxxRT290-S0200, CREE Inc.).

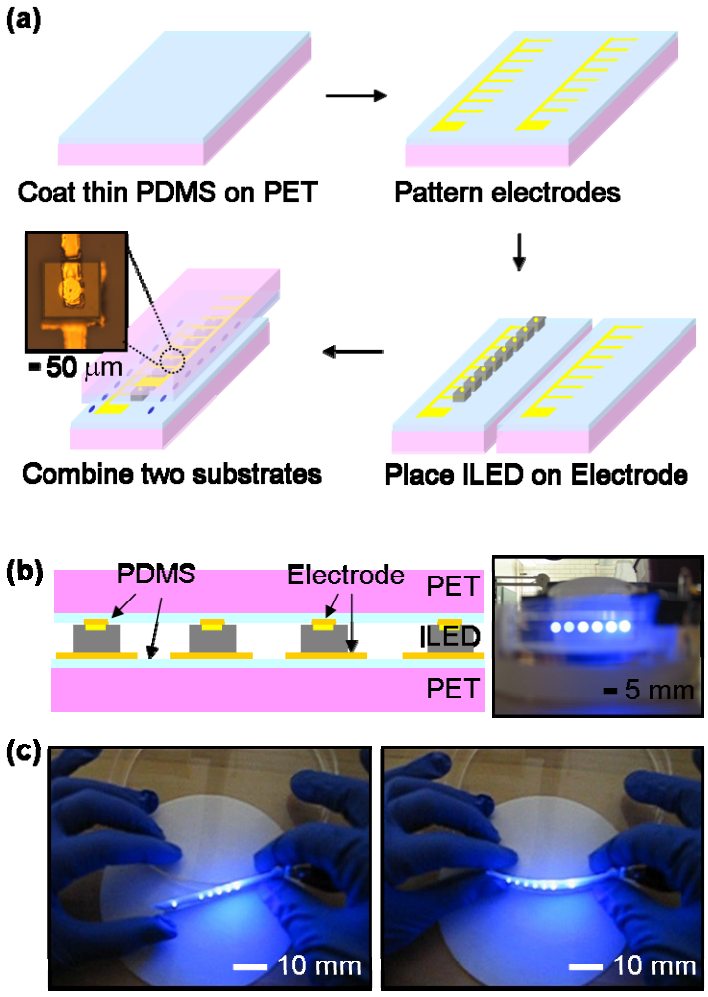


Figure 5.2 (a) Schematic process flow for fabricating a ILEDs strip lighting system. (b) Schematic cross sectional geometry of the strip lighting system and optical image of the strip light in operation at $R = 60$ mm. (c) Optical images of the strip light in operation during repeatable bending ($R = 60$ mm) and releasing ($R = \infty$) cycles.

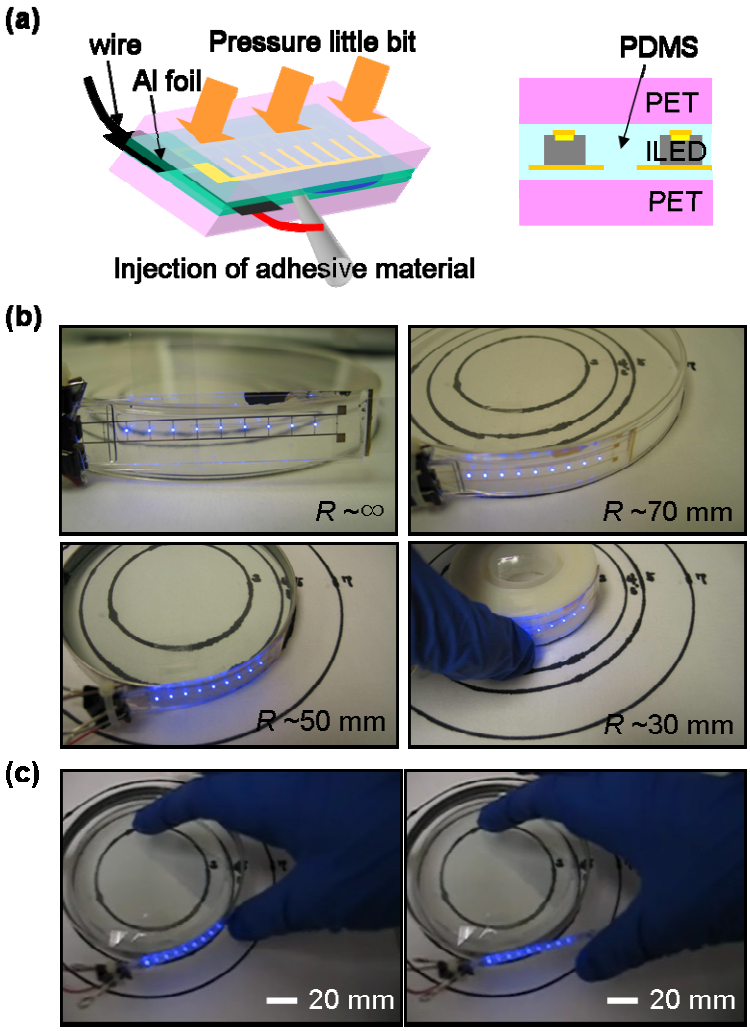


Figure 5.3 (a) Schematic illustration of injection of adhesive materials (PDMS) in the strip lighting system. (b) Optical images of the strip light filled with PDMS in operation at $R = \infty$, 70, 50, and 30 mm. (c) Optical images of the strip light filled with PDMS in operation during repeatable bending (R = 50 mm) and releasing ($R = \infty$) cycles.

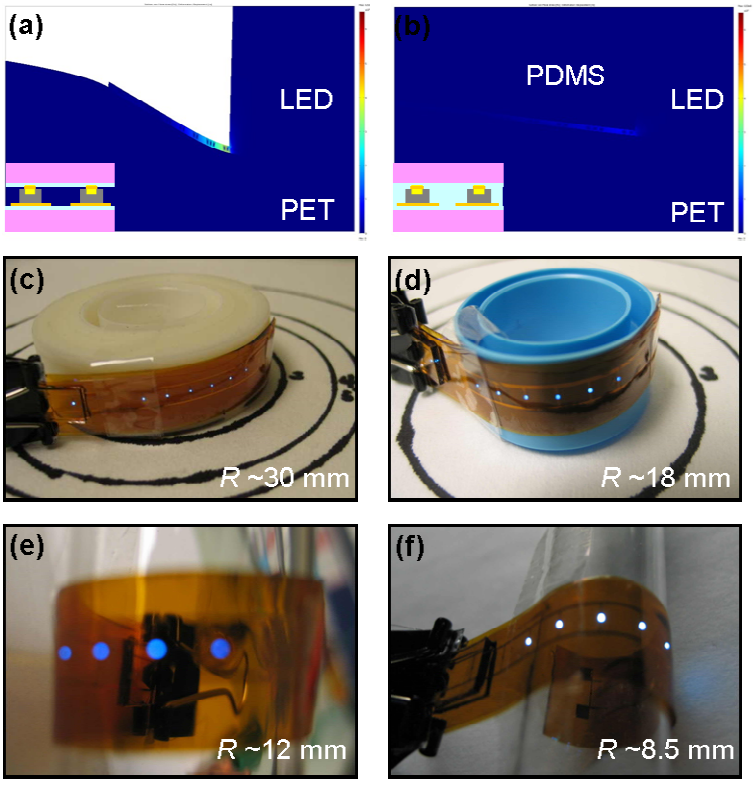
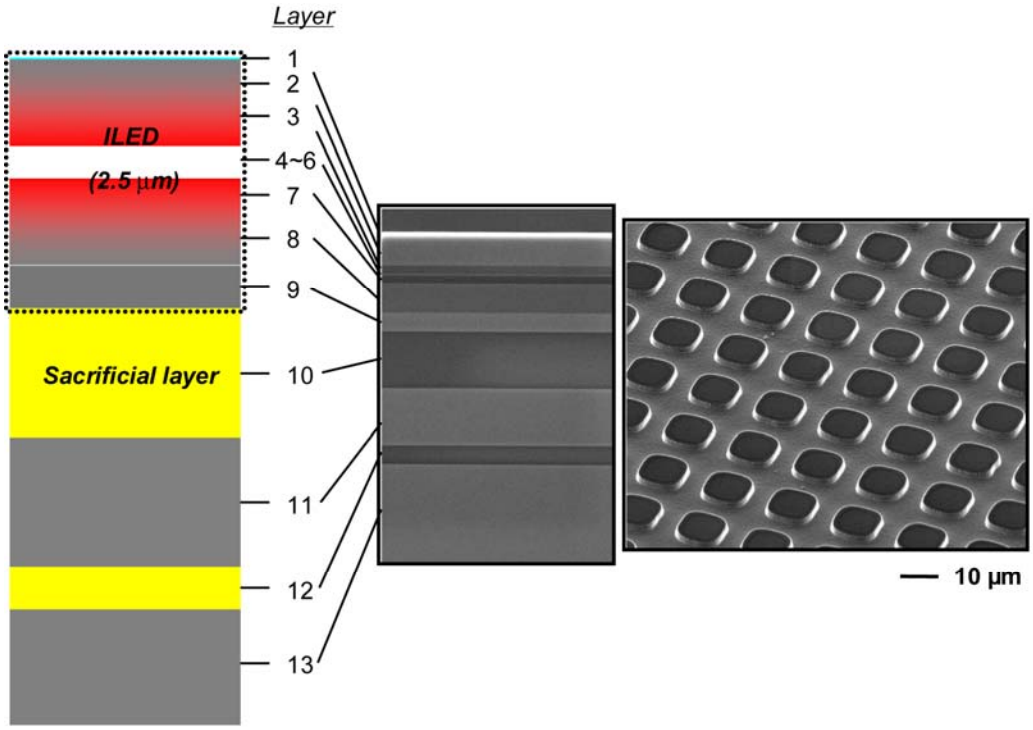


Figure 5.4 Finite element analysis in cases of the ILEDs strip light systems with (a) open and (b) filled structures. Optical images of the strip light on thin top and bottom polyimide (PI) substrates (~100 μm thick) in operation at R = (c) 30 mm, (d) 18 mm, (e) 12 mm, and (f) 8.5 mm, respectively.



Layer	Layer Name	Material	Thickness (nm)	Type	Dopant	Concentration (cm^{-3})
1	Contact	GaAs	5	P	C	1.00E+19
2	Spreader	$Al_{0.45}Ga_{0.55}As$	800	P	C	1.00E+18
3	Clad	$In_{0.5}Al_{0.5}P$	200	P	Zn	3E17 to 6E17
4	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
5	Well	$In_{0.56}Ga_{0.44}P$	6	-	-	<1E16
6	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
7	Clad	$In_{0.5}Al_{0.5}P$	200	N	Si	1.00E+18
8	Spreader	$Al_{0.45}Ga_{0.55}As$	800	N	Si	1.00E+18
9	Contact	GaAs	500	N	Si	4.00E+18
10		$Al_{0.96}Ga_{0.04}As$	1500	N	Si	1.00E+17
11		GaAs	1500	N	Si	1.00E+17
12		$Al_{0.96}Ga_{0.04}As$	500	N	Si	1.00E+17
13	Substrate	GaAs		N	Si	>1E18

Figure 5.5 Schematic illustration (left) and cross sectional SEM image (middle) of the epitaxial semiconductor multilayer stack on a GaAs wafer. (Right) SEM image of a square array of laterally delineated, square ILEDs on a GaAs wafer. (Bottom) Details of the epi-stack.

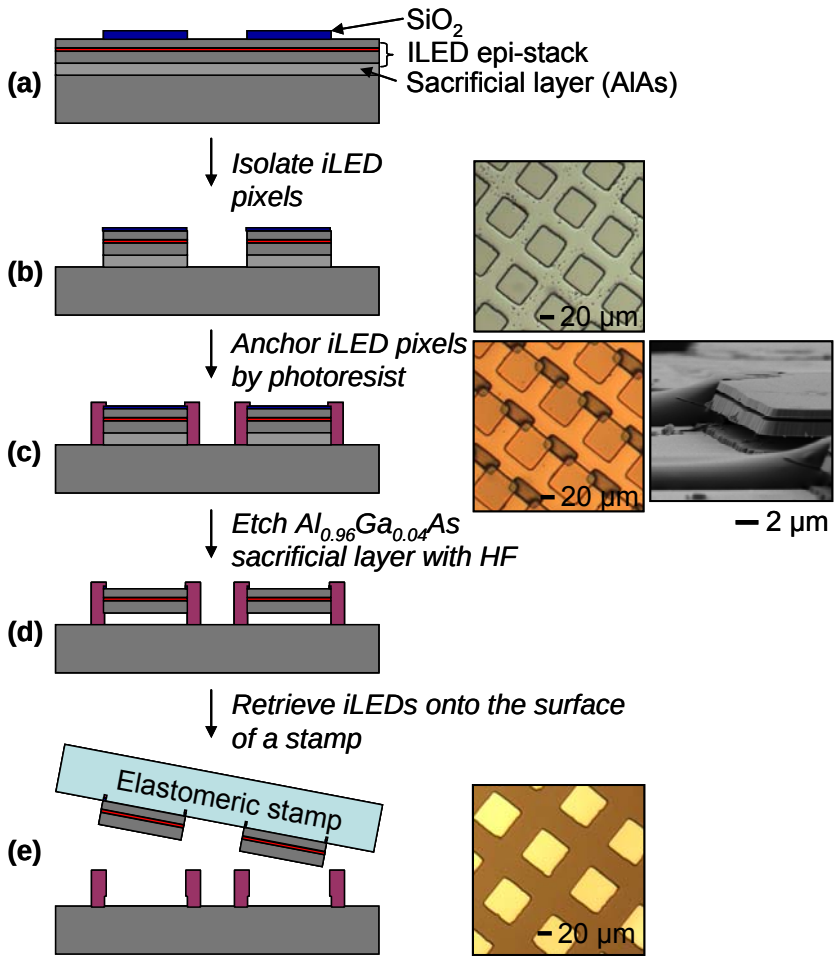


Figure 5.6 Schematic illustration and optical microscope/SEM images of processing steps for retrieving ILEDs from a GaAs source wafer.

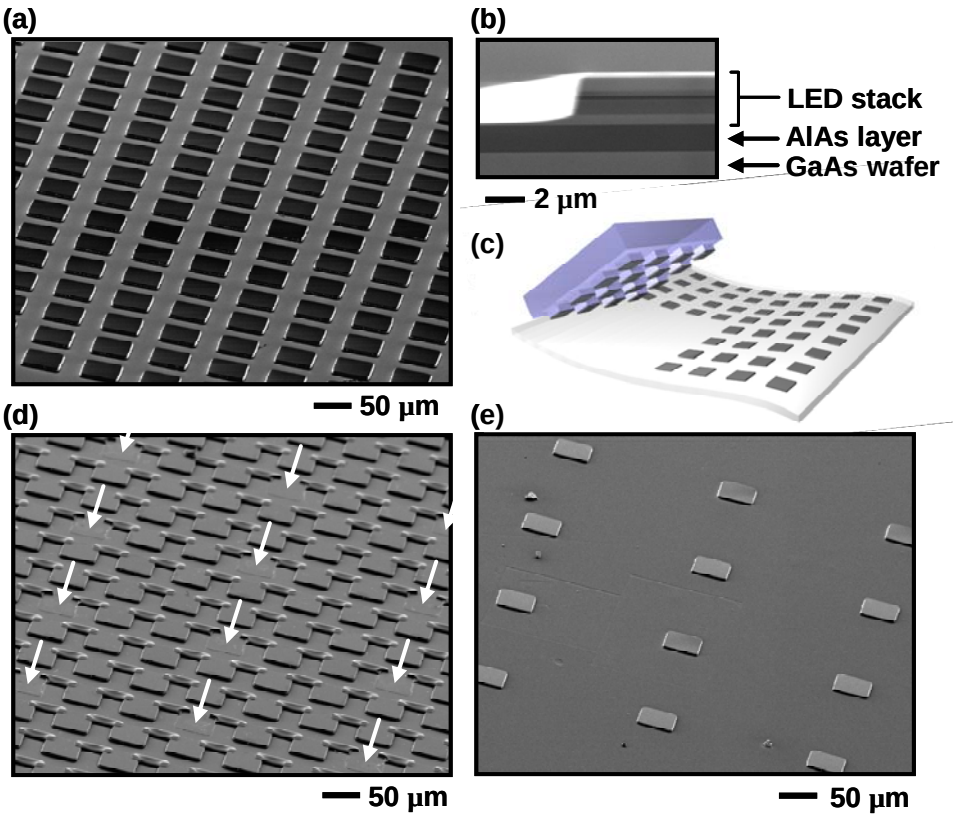


Figure 5.7 (a) SEM image of a square array of AlInGaP LED structures (50x50 μm) created by vertical, patterned etching through an epitaxial multilayer stack grown on a GaAs wafer. (b) Cross sectional SEM view of one of these structures, showing the LED semiconductor layers (quantum wells, as well as cladding, spreading and contact layers) on a sacrificial epilayer of AlAs. (c) Schematic illustration of a printing based assembly method for transferring collections of LEDs (gray) released from the GaAs wafer to a target substrate (shown here as a flexible sheet). (d) SEM image of the GaAs wafer after removing a set of LEDs (indicated by white arrows) with a stamp. (e) SEM image of a region of the target substrate printed with this stamp.

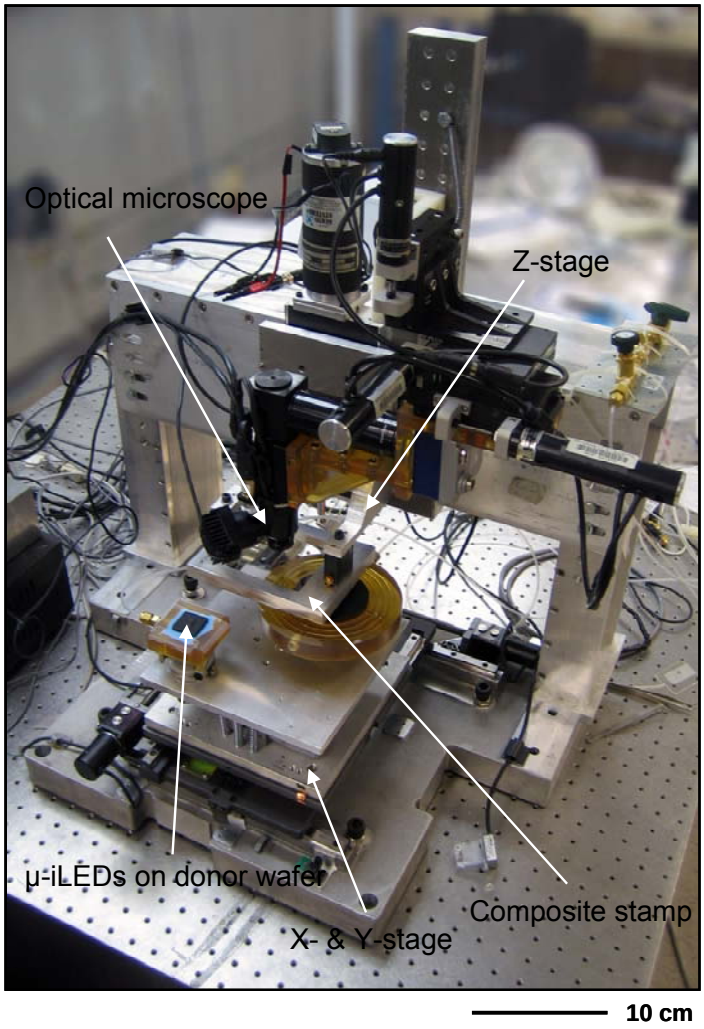


Figure 5.8 Picture of the automated printing machine, with key parts labeled.

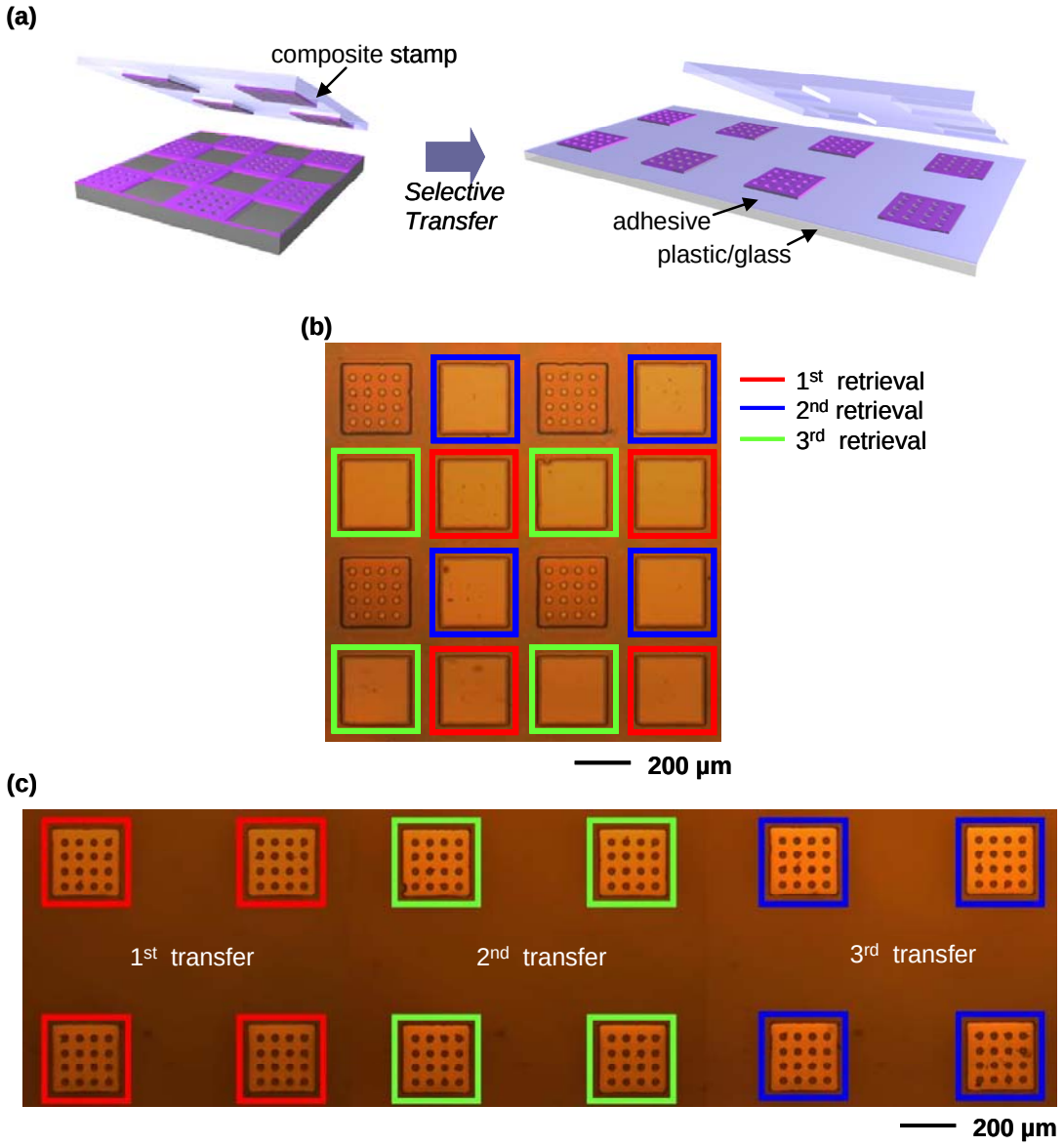


Figure 5.9 (a) Schematic illustration of retrieving and printing selected sets of ILEDs with a composite stamp. (b) Optical microscope image of the source wafer after three cycles of printing. (c) Optical microscope image of a substrate with sparsely printed ILEDs derived from the source wafer of (B), illustrating the concept of area expansion.

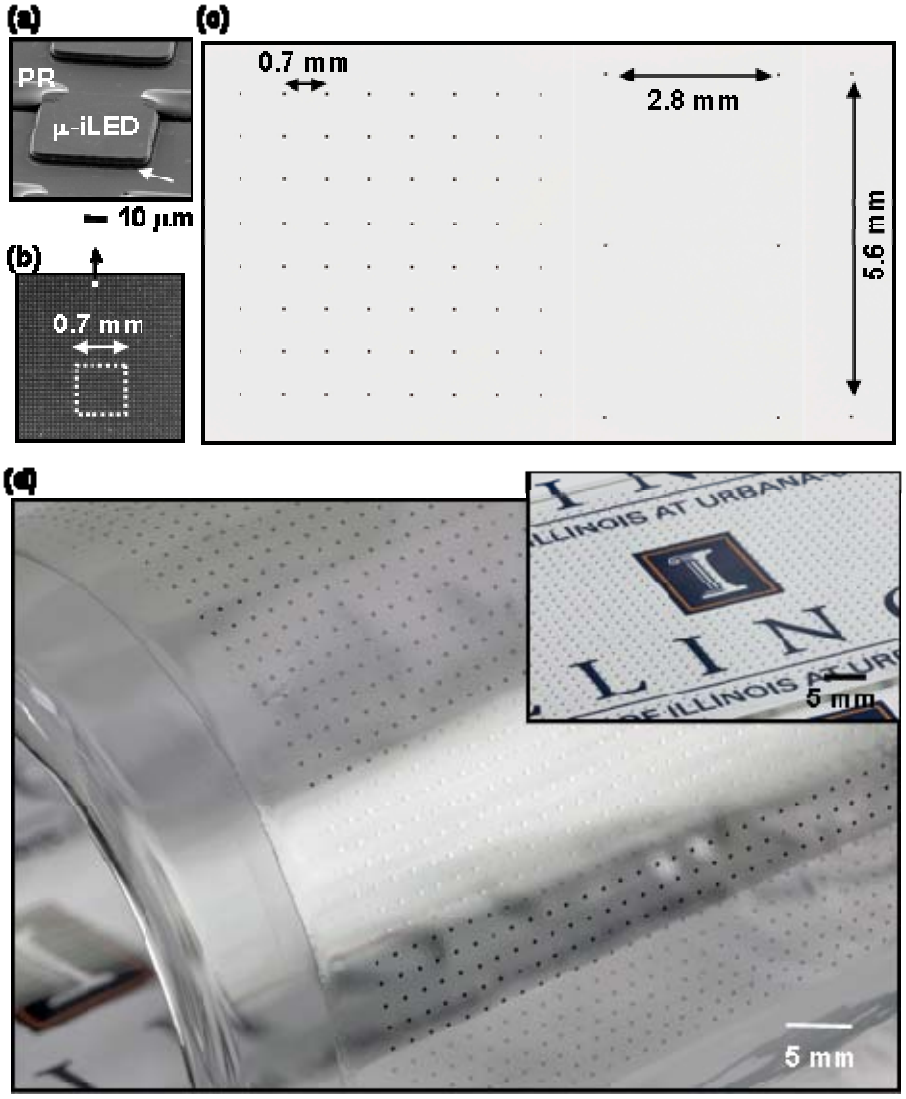


Figure 5.10 (a) Angled view SEM image of an individual LED (i.e. ILED) from the array in Fig. 5.7d. A pair of 'breakaway' photoresist (PR) anchors at the two far corners of the device holds it above the GaAs wafer in the suspended configuration of a diving board, for ease of liftoff with a stamp. The white arrow points to the region of removed AlAs. (b) SEM image of a dense collection of such devices on a piece of a GaAs wafer. The black arrow and white dot indicate, roughly, the region of this chip that corresponds to the image of (adevices at different spacings, derived from the chip shown in (b). (d) Large scale collection of ILEDs (1600 Devices, in a square array with pitch of 1.4 mm) printed onto a thin, flexible sheet of plastic, shown here wrapped onto a cylindrical glass substrate (main frame). The inset shows a similar collection of ILEDs (1600 Devices, in a square array with pitch of 1.4 mm) printed onto a plate of glass. For these cases, relatively large ILEDs were selected for ease of viewing; devices with dimensions of Fig. 5.7e are invisible at this magnification.

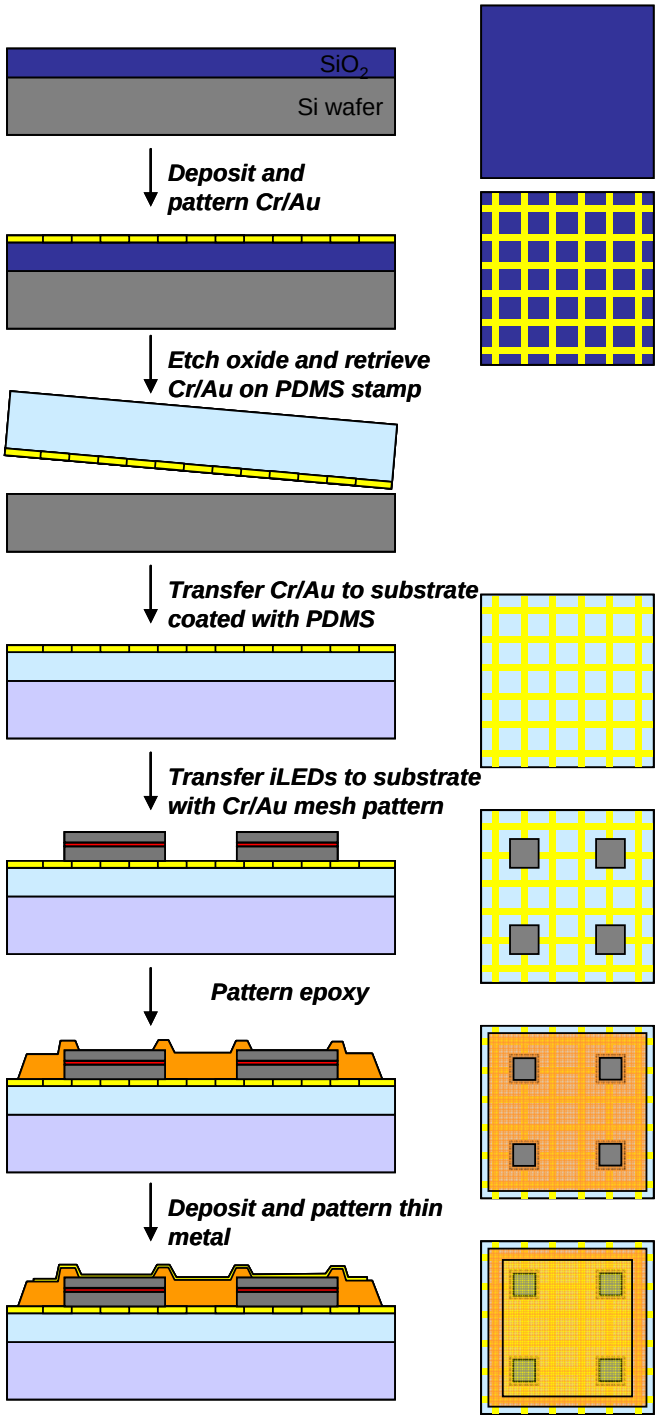


Figure 5.11 Schematic illustration of processing steps for fabricating an array of small ILEDs (25 μm × 25 μm) contacted by a metal (Au) mesh.

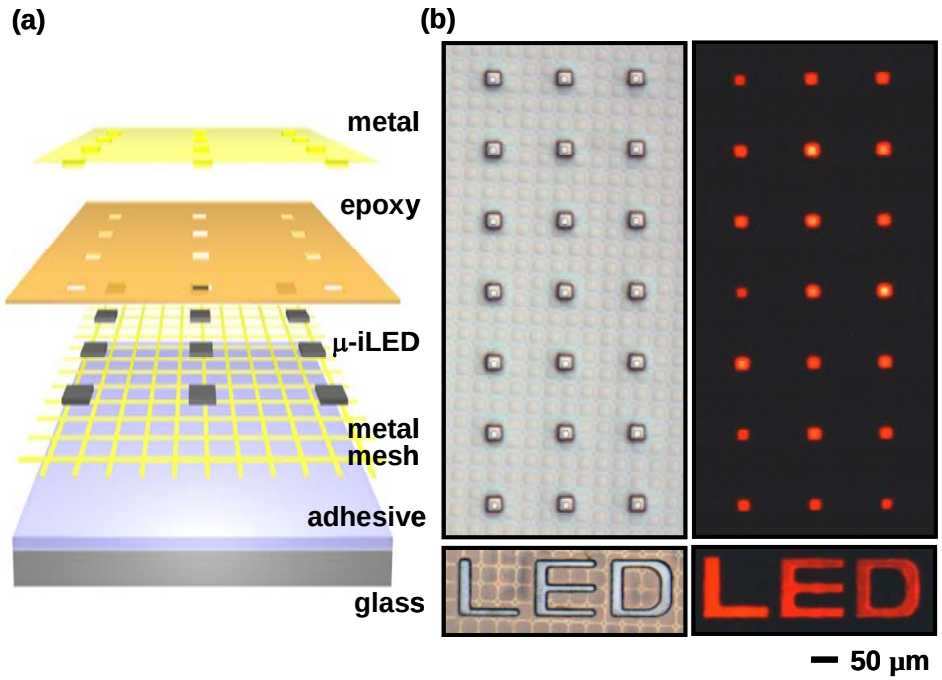


Figure 5.12 (a) Exploded view schematic illustration of an array of ILEDs contacted by a metal mesh (bottom; n contacts) and a metal film (top; p contacts). A thin adhesive layer of PDMS facilitates printing onto the glass substrate. A photopatterned layer of epoxy on top of the devices prevents shorting of the top film to the bottom mesh. (b) Optical micrographs of an array of ILEDs (top: 25 μm x25 μm, square geometries; bottom: characters 'LED') in their off state with frontside illumination (left) and in their on state without illumination (right).

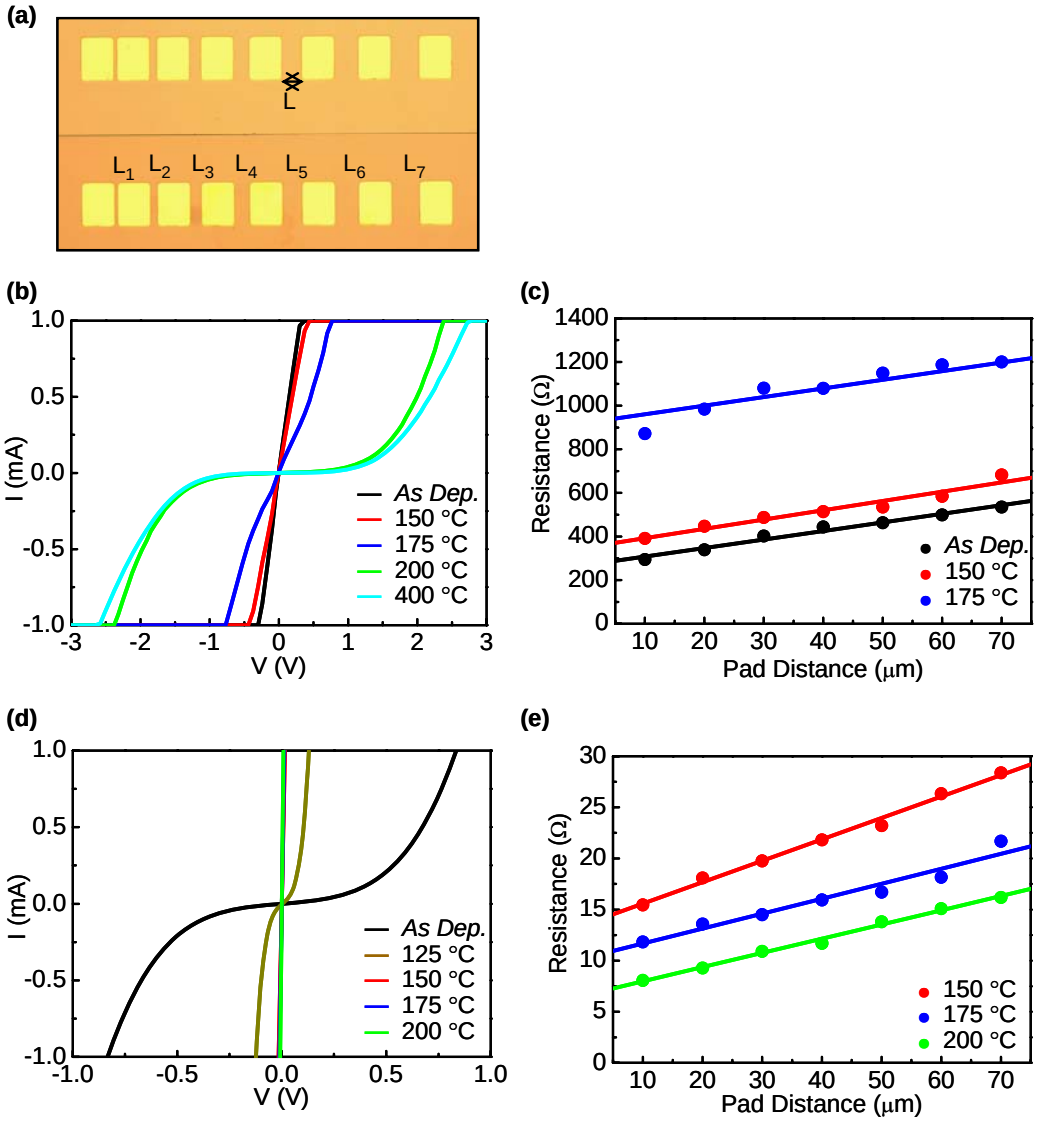


Figure 5.13 (a) Optical microscope image of transmission line model (TLM) patterns with gaps of L_1 = 10 μm, L_2 = 20 μm, L_3 = 30 μm, L_4 = 40 μm, L_5 = 50 μm, L_6 = 60 μm, L_7 = 70 μm. (b) I (current) – V (voltage) curves associated with p contacts (Pt/Ti/Pt/Au = 10/40/10/70 nm) as a function of annealing temperature. (c) Resistance as a function of gap length, for the p contact metallization, evaluated at different annealing temperatures. (d) I-V curves associated with n contacts (Pd/Ge/Au = 5/35/70 nm) as a function of annealing temperature. (e) Resistance as a function of gap length, for the n contact metallization, evaluated at different annealing temperatures.

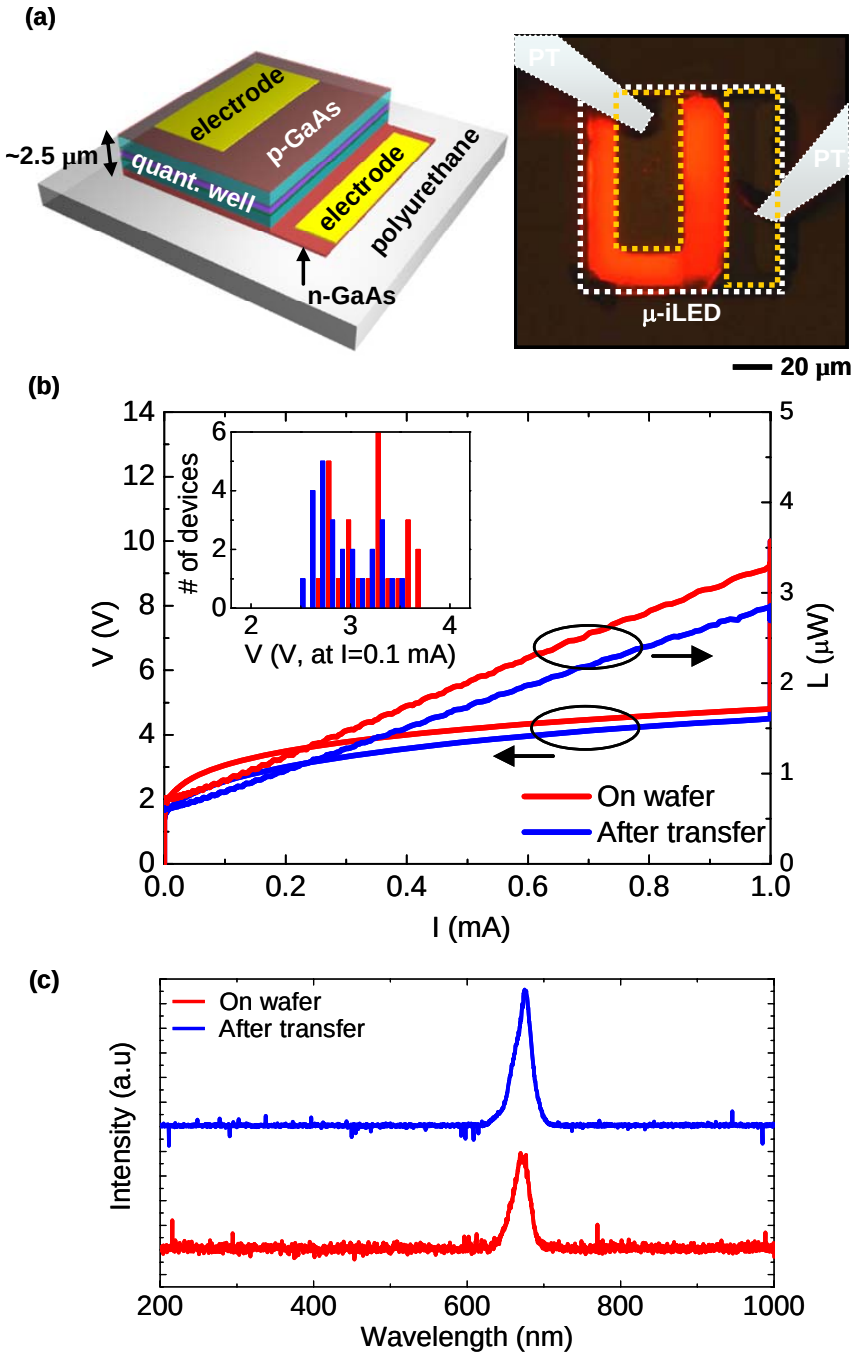


Figure 5.14 (a) Schematic illustration of an ILED with ohmic contacts (left) and optical image of an operating device (right), showing uniform emission at all regions. (b) Current-voltage-emission characteristics of a device before undercut etching and after transfer printing. Inset: a histogram of the bias voltages needed to produce currents of 0.1 mA in a collection of devices. (c) Spectral characteristics of emission for a typical device on the wafer and after transfer printing.

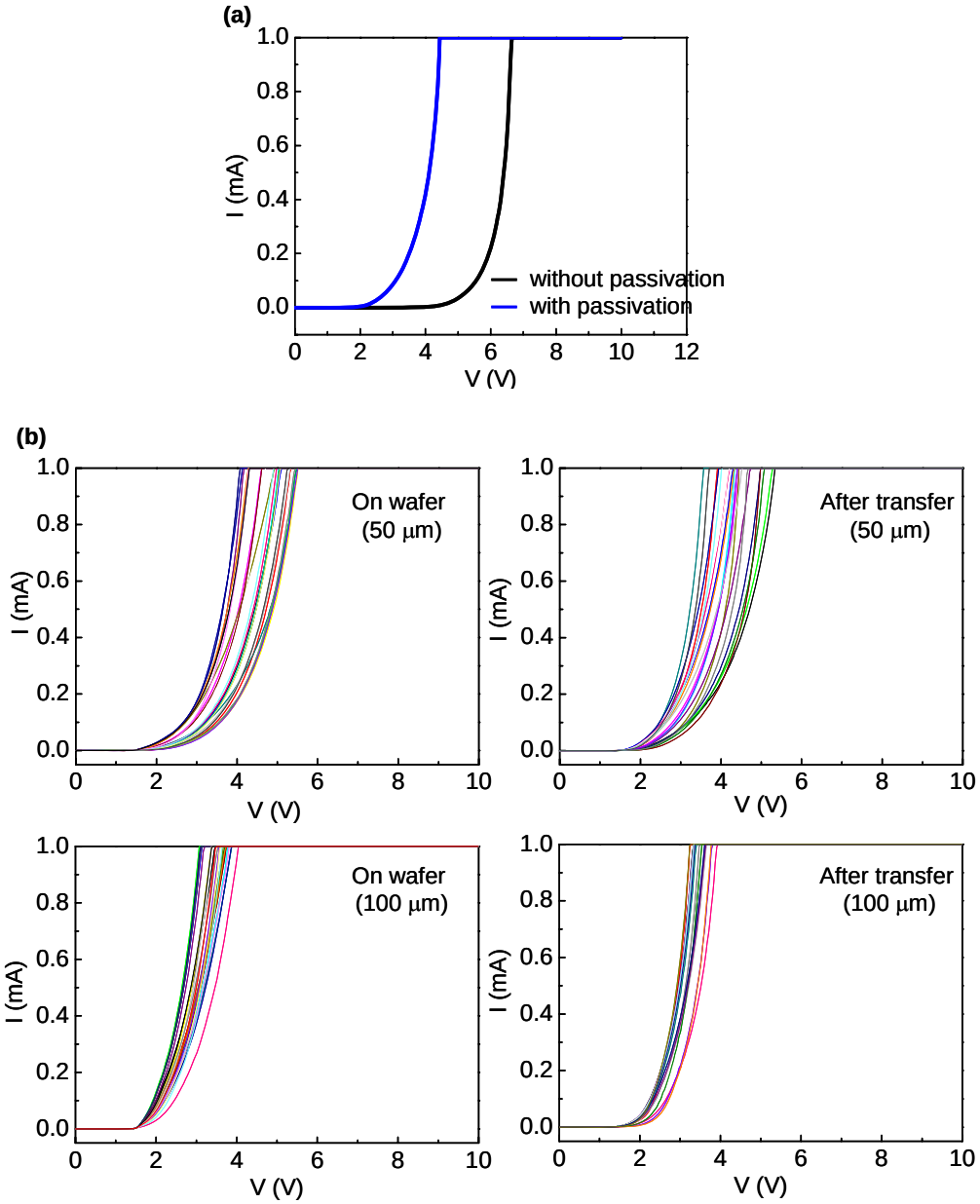


Figure 5.15 (a) I-V curves of ILED devices with ohmic contacts with and without a passivation scheme to protect the sidewalls during undercut etching. (b) I-V curves of ILED devices (50 μm x 50 μm and 100 μm x 100 μm) with ohmic contacts and passivation scheme, before and after transfer.

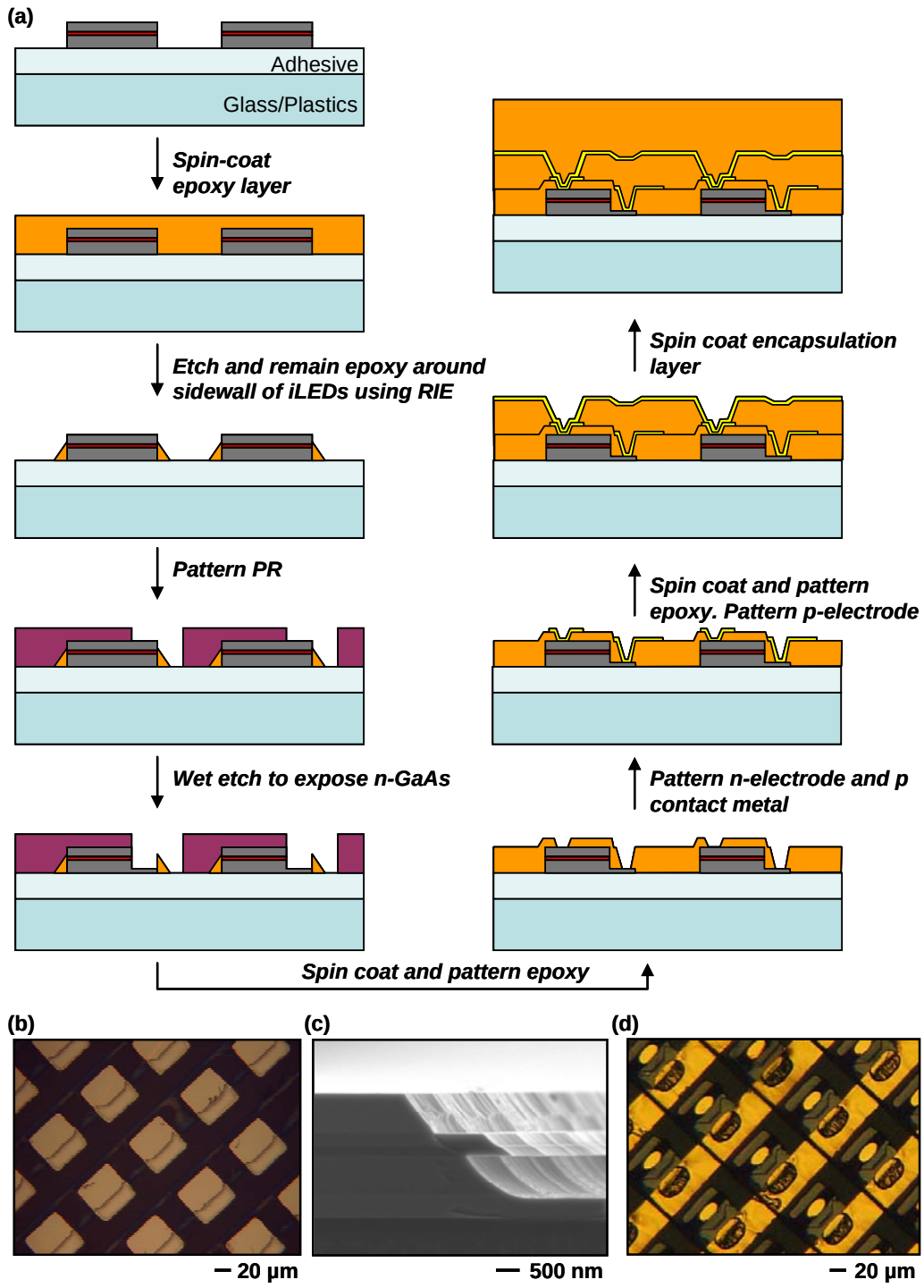


Figure 5.16 (a) Schematic illustration of processing steps for fabricating electrical interconnections to complete a passive matrix array. (b) Optical microscope image of an array of ILEDs array after exposing n-GaAs by wet etching. (c) Cross sectional SEM view of an ILED after exposing n-GaAs by wet etching. (d) Optical microscope image of an array of ILEDs array with electrical interconnections.

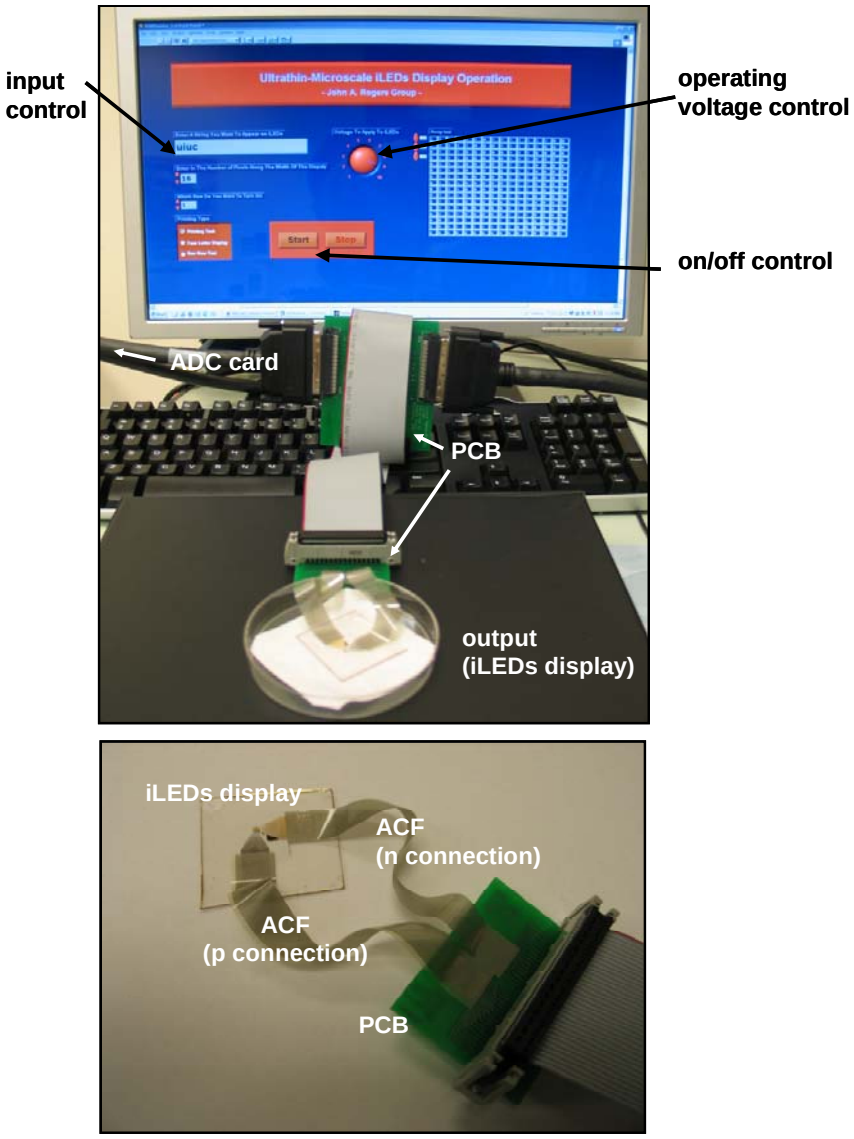


Figure 5.17 Pictures of the operating interface, anisotropic conductive film (ACF) ribbon cables and printed circuit boards (PCBs) for computer control.

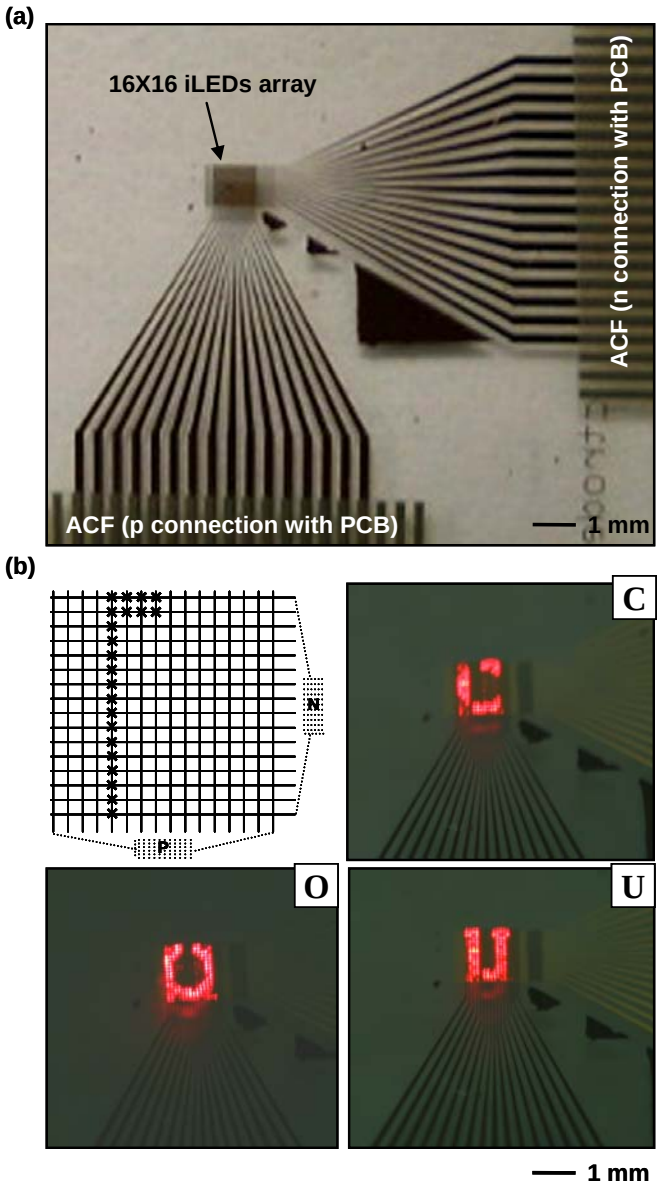


Figure 5.18 (a) Optical image of a 16x16 ILED (50 μm x 50 μm with a pitch of 70 μm) display on a glass substrate with ACF ribbon cable connection. (b) Optical images of the display during the operation. (Left-top) a map of non-working pixels (indicated by 'x' symbols).

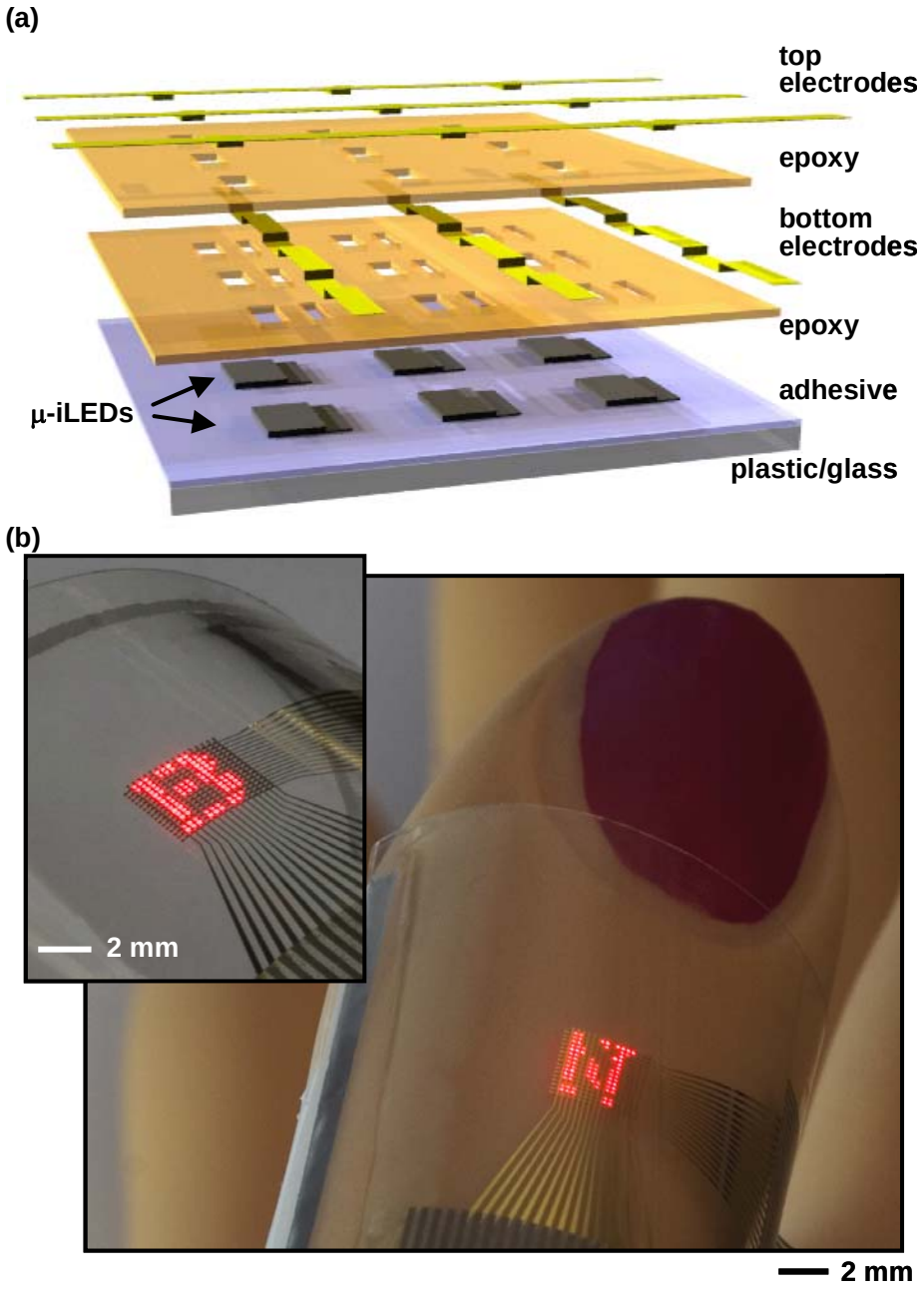


Figure 5.19 (a) Schematic illustration of a planar scheme for interconnecting a printed array of ILEDs in a passive matrix layout.. (b) Images of a flexible display that incorporates a 16x16 array of ILEDs in the layout shown in (a), on a sheet of plastic (PET), wrapped around the thumb of a mannequin hand (main frame; human scale; radius ~8 mm) and a cylindrical glass tube (inset; radius ~12 mm). External interface to control electronics occurs through ribbon cables bonded to column and row electrodes that emerge from the periphery of the display.

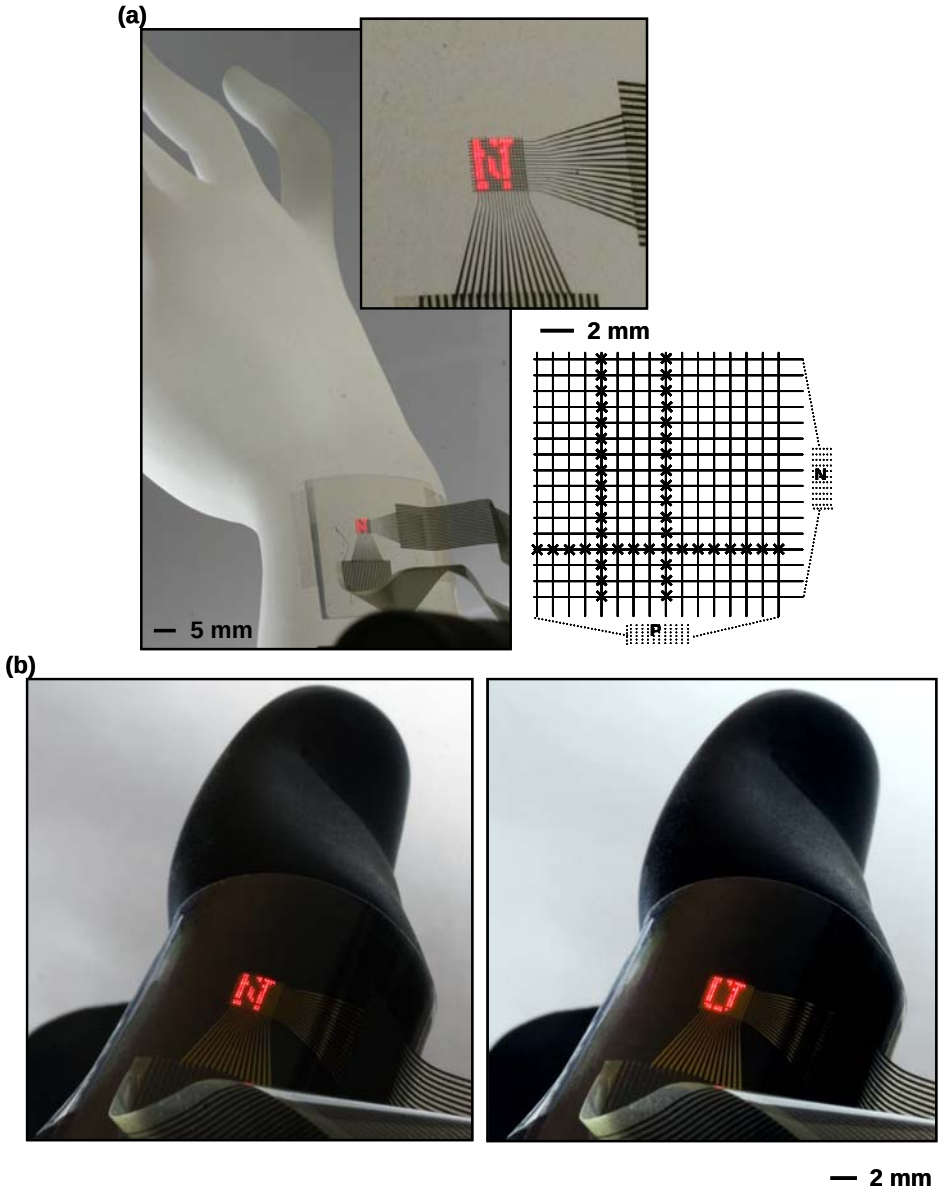


Figure 5.20 Optical images of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate, wrapped onto the wrist (a) and finger (b, c) of manikin. (Bottom right) a map of non-working pixels (indicated by 'x' symbols).

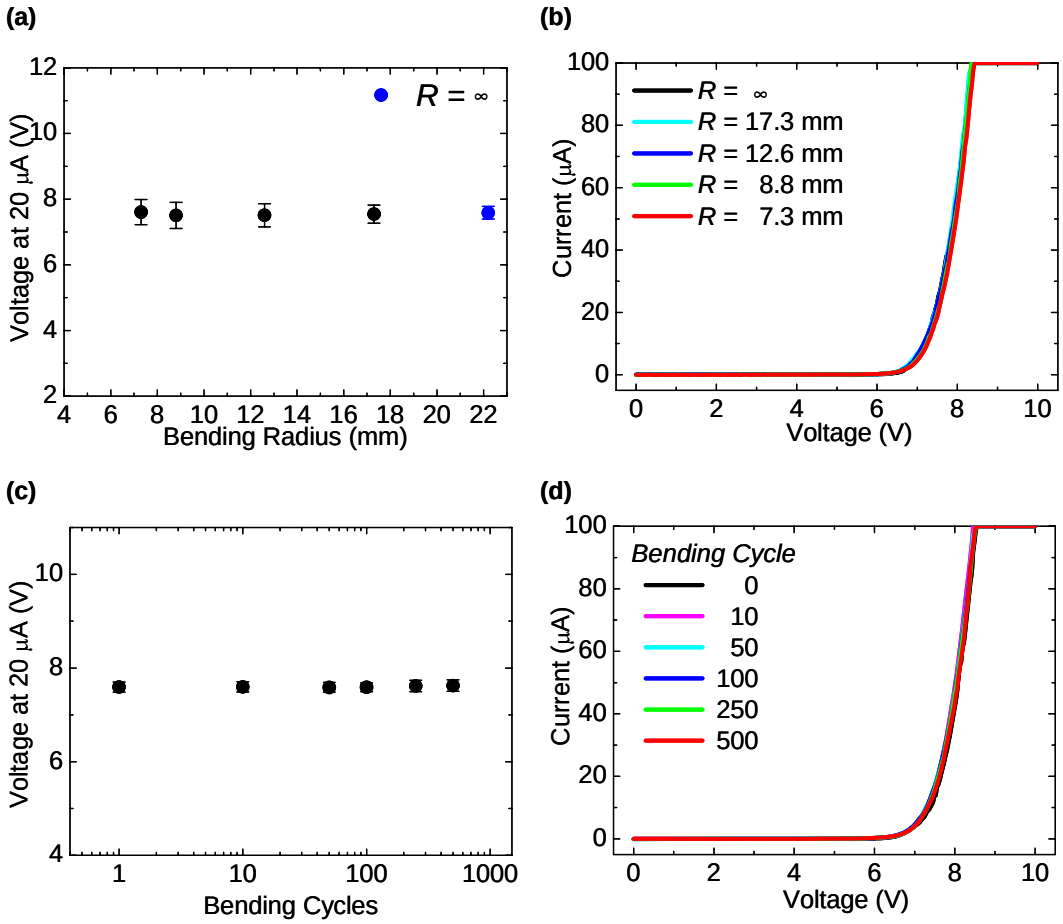


Figure 5.21 Electrical properties of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate. (a) Plot of voltage at 20 μA and (b) I-V curves under $R = \infty$, 17.3, 12.6, 8.8, 7.3 mm. (c) Plot of voltage at 20 μA and (d) I-V curves as a function of bending cycles up to 500 times at R = 8.8 mm. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

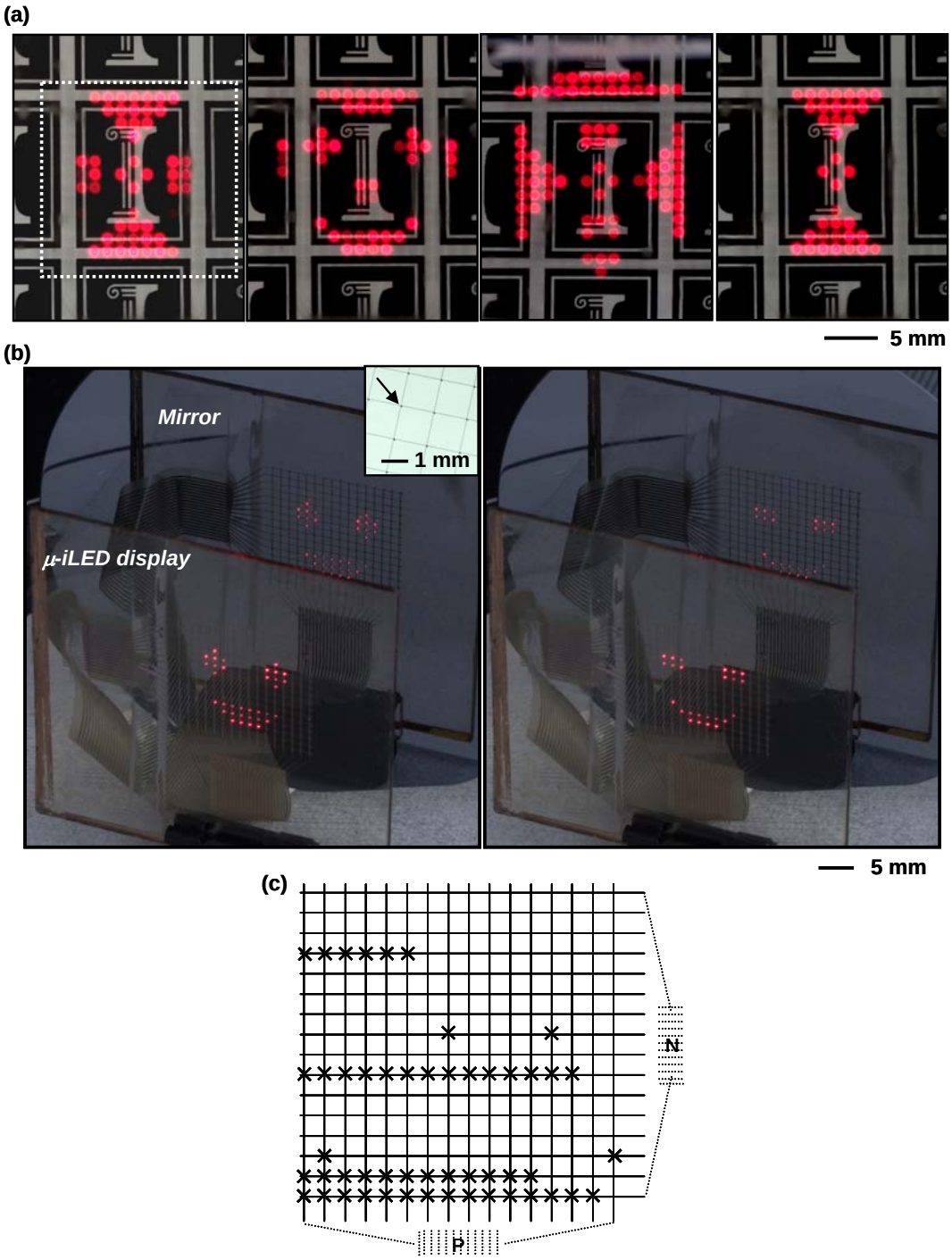


Figure 5.22 **(**a) Optical images of a comparatively large, semitransparent 16x16 ILEDs display (100 μm x 100 μm with a pitch of 1.20 mm) on a glass substrate. (b) Optical images of a similar device (bottom left) displaying a different pattern in front of a mirror (upper right), to illustrate the bidirectional emission property. Inset: a magnified view of a region of the display in its off state, to illustrate the small areal coverage of the devices. (c) A map of non-working pixels (indicated by 'x' symbols).

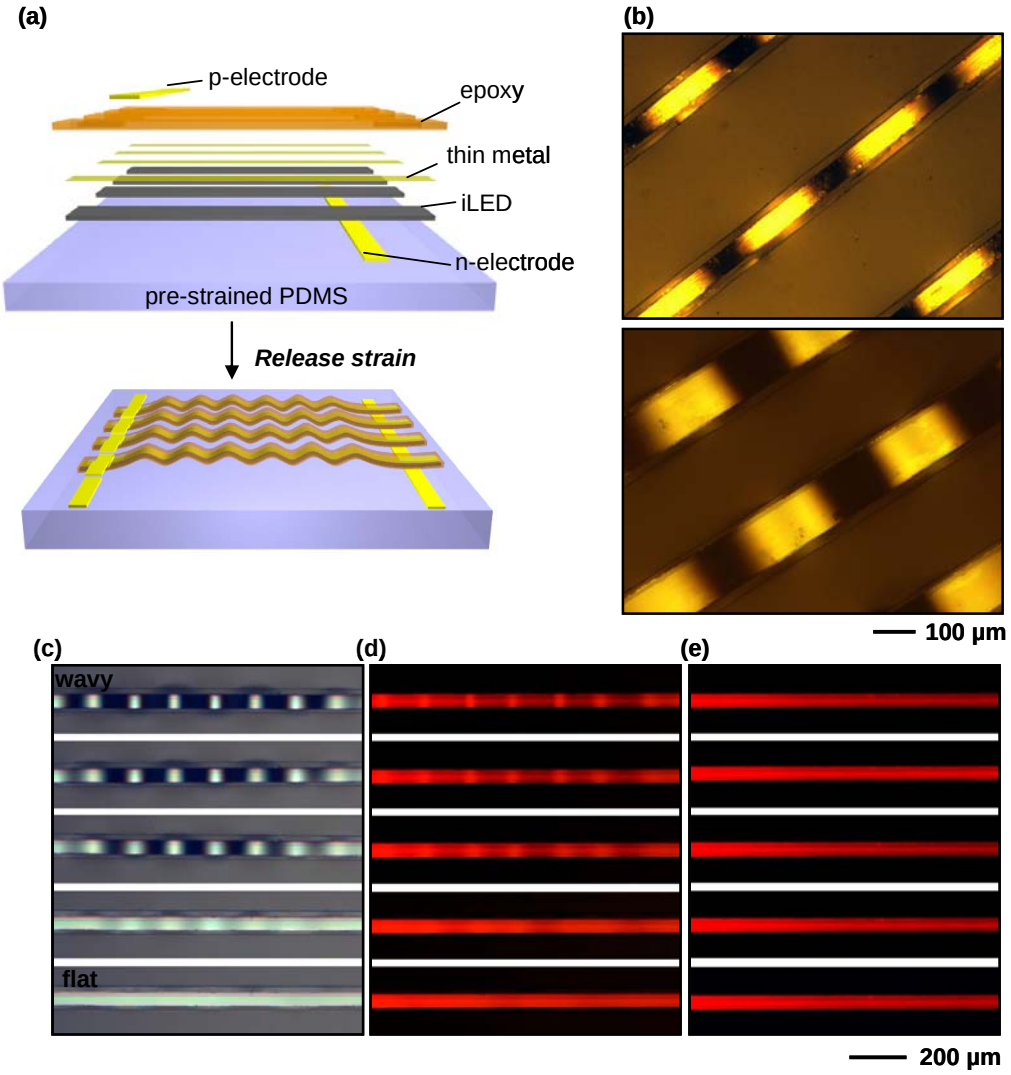


Figure 5.23 (a) Exploded schematic illustration of processing steps for wavy ILEDs ribbons. (b) Optical microscope image of wavy ILEDs ribbons with 50 μm and 100 μm width collected with a scanning focal technique. Optical microscope image of a wavy ILEDs ribbon in different strained states (from wavy to flat): (c) non-emission with illumination, (d) emission with illumination, (e) emission without illumination.

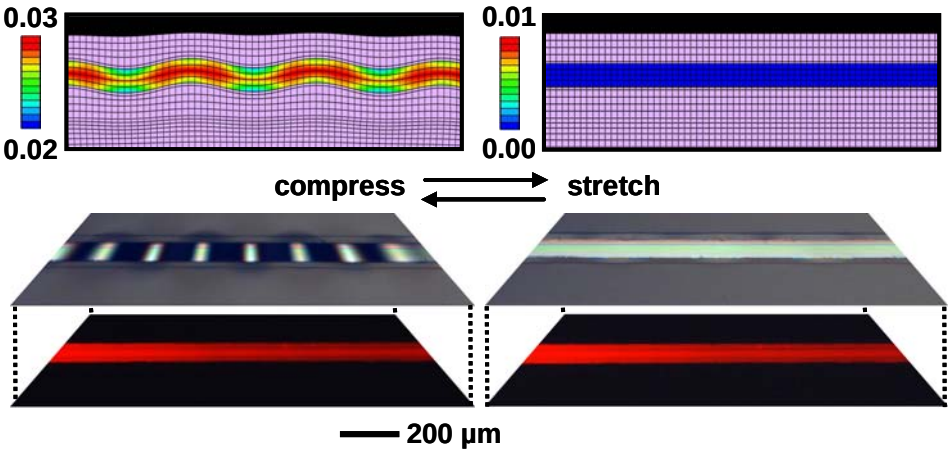


Figure 5.24 Color plots of the strain distributions (in percent) at the quantum well region and the corresponding finite element mesh used for simulation (top) and optical micrographs (bottom) of a stretchable ILED on a rubber substrate in unstrained and strained states. The upper and lower images in the bottom frames show illuminated, reflection mode micrographs and micrographs of the emission without illumination, respectively.

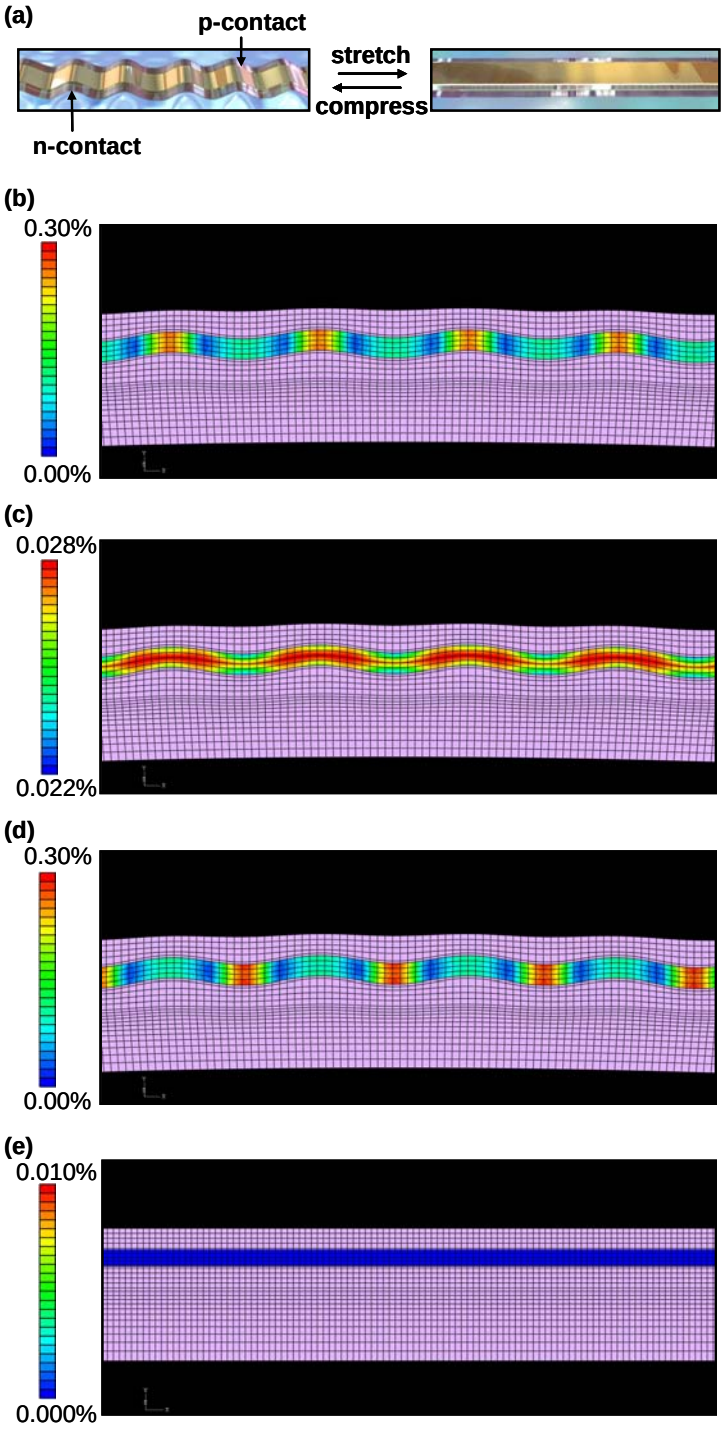


Figure 5.25 (a) Schematic illustrations of a stretchable ILED on a rubber substrate in compressed (left) and stretched (right) configurations. Strain distributions in the device: (b) top surface, (c) middle surface (quantum well region), (d) bottom surface in a compressed state and (e) middle surface in a stretched state.

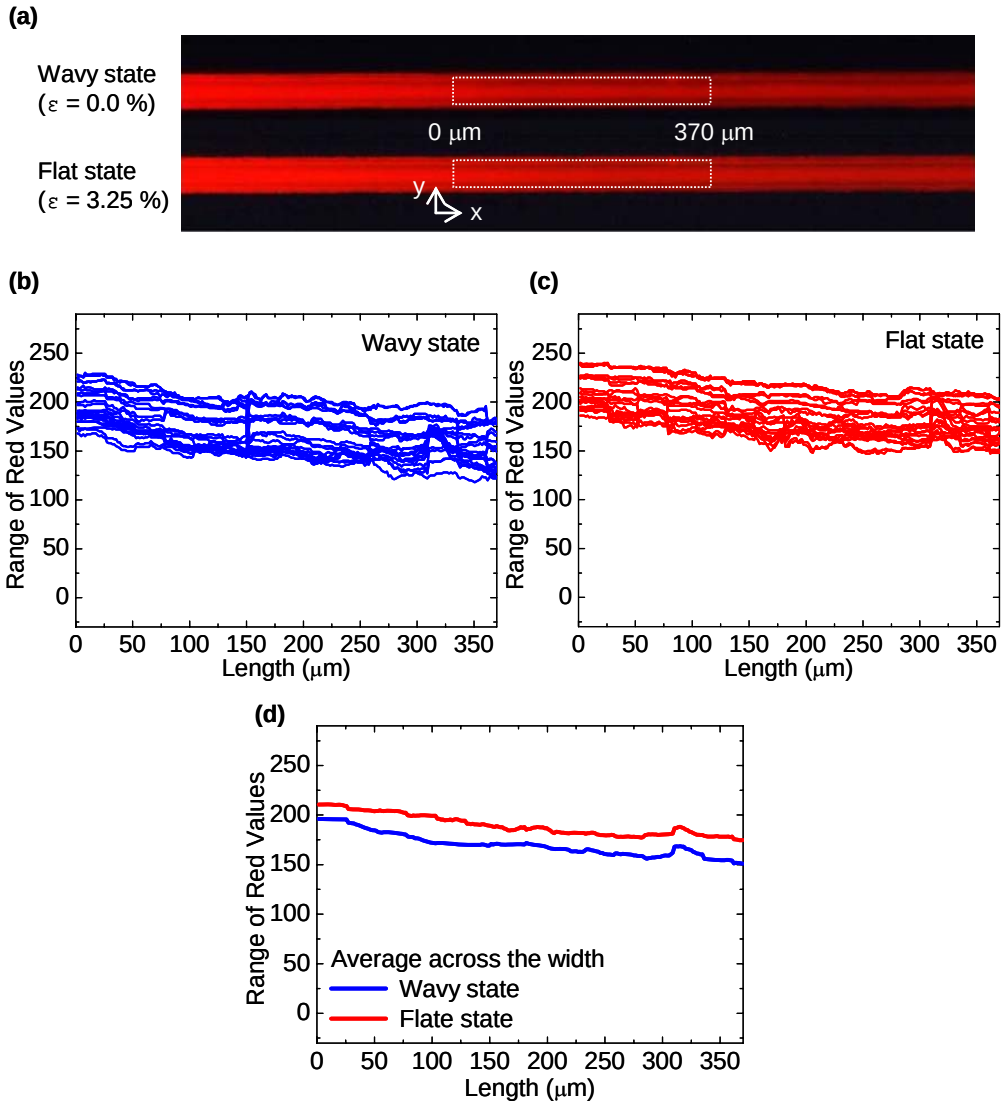


Figure 5.26 (a) Optical microscope images of emission, collected without illumination, from wavy ILEDs ribbons in wavy (top) and flat (bottom) configurations. Color analysis of pixels recorded in white square box of (a) using a utilities available in a commercial software package (Photoshop, Adobe Systems): range of red values of emission from (b) the wavy and (c) flat configurations, as a function of position along the ribbon length (0 = white, 255 = full red). (d) Averaged range of red values of emission across the ribbon width from (b) and (c).

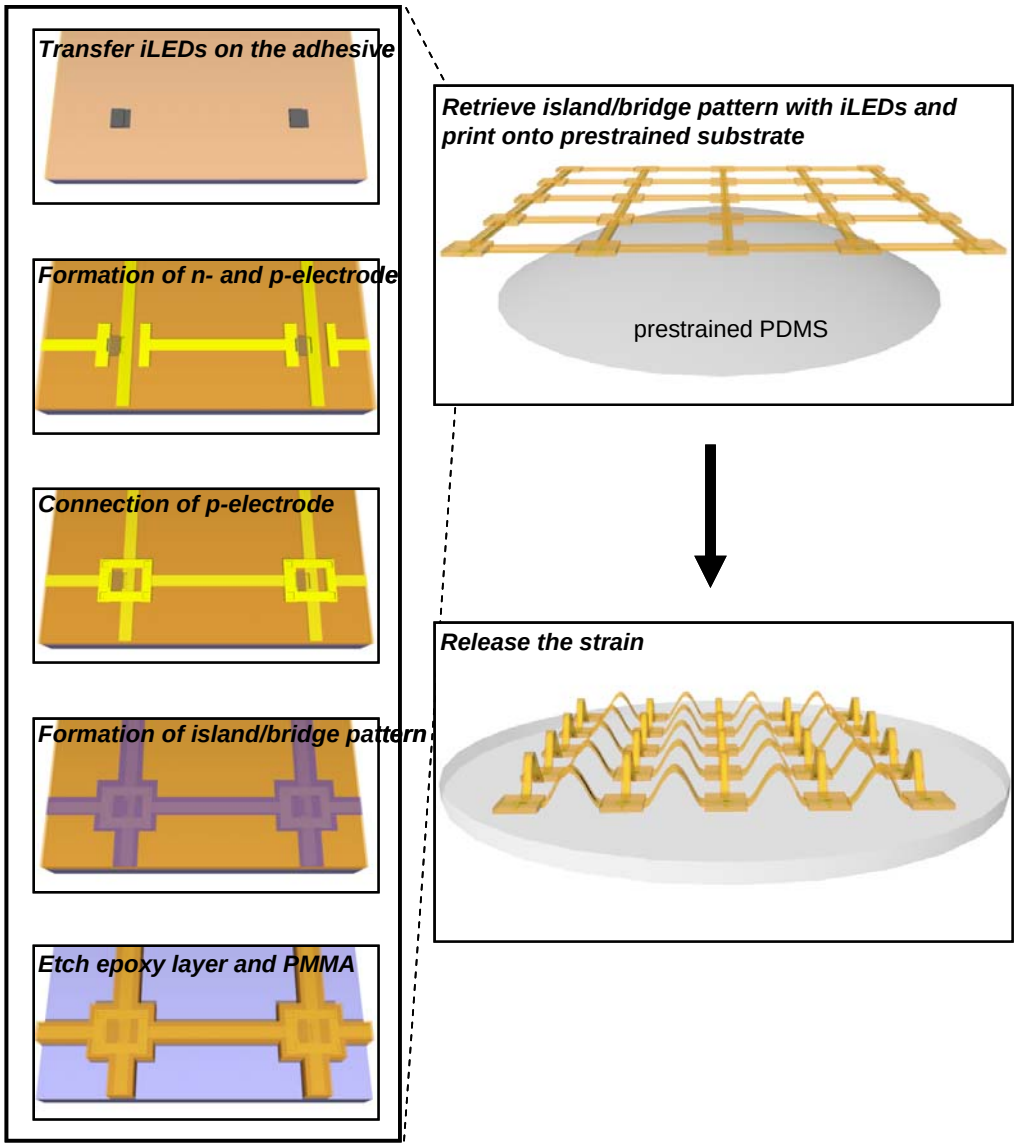


Figure 5.27 (a) Schematic illustration of processing steps for fabricating stretchable ILEDs display. (b) A map of non-working pixels (indicated by 'x' symbols).

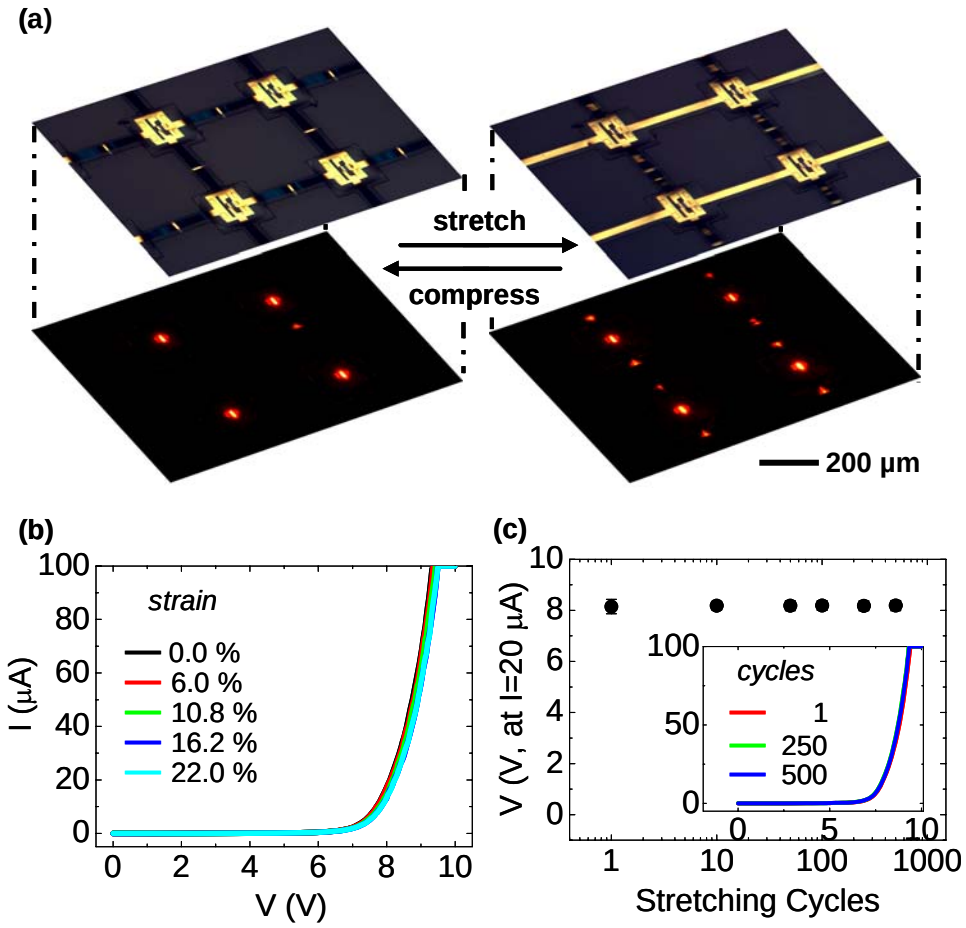


Figure 5.28 (a) Optical micrographs of a set of four pixels in the display shown in (a). The upper and lower images in the bottom show illuminated, reflection mode micrographs and micrographs of the emission without illumination, respectively. (b) Current (I) / voltage (V) measurements on a representative ILED in the display, at different applied strains. (c) Voltage (V) needed to generate a current of 20 μA measured after stretching cycles to 500 times at an applied strain of 22%. The inset shows the I-V behavior after these cycling tests. These devices have relatively high turn on voltages, due to the use of non-ohmic contacts.

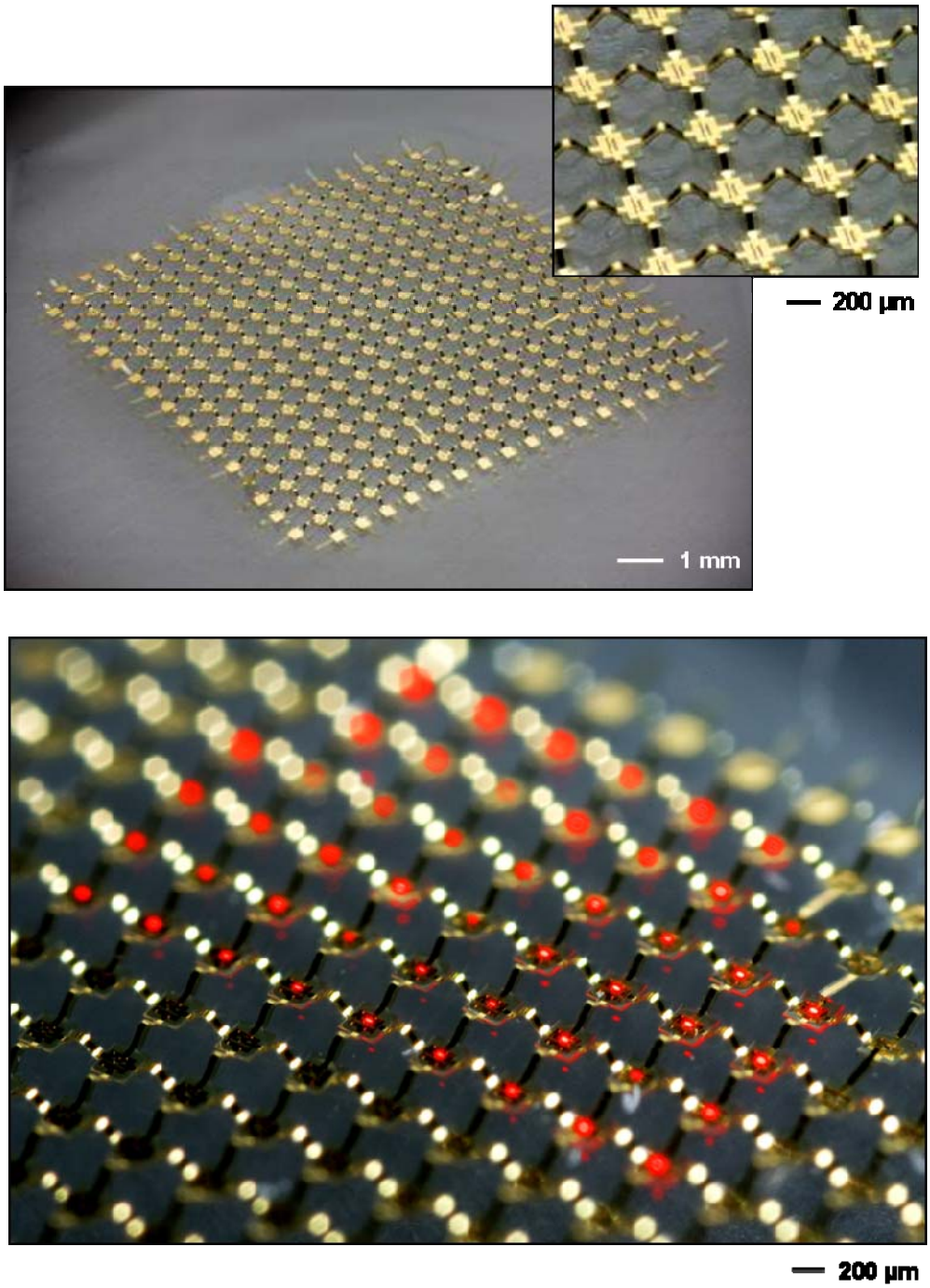


Figure 5.29 Optical microscope images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a flat rubber substrate.

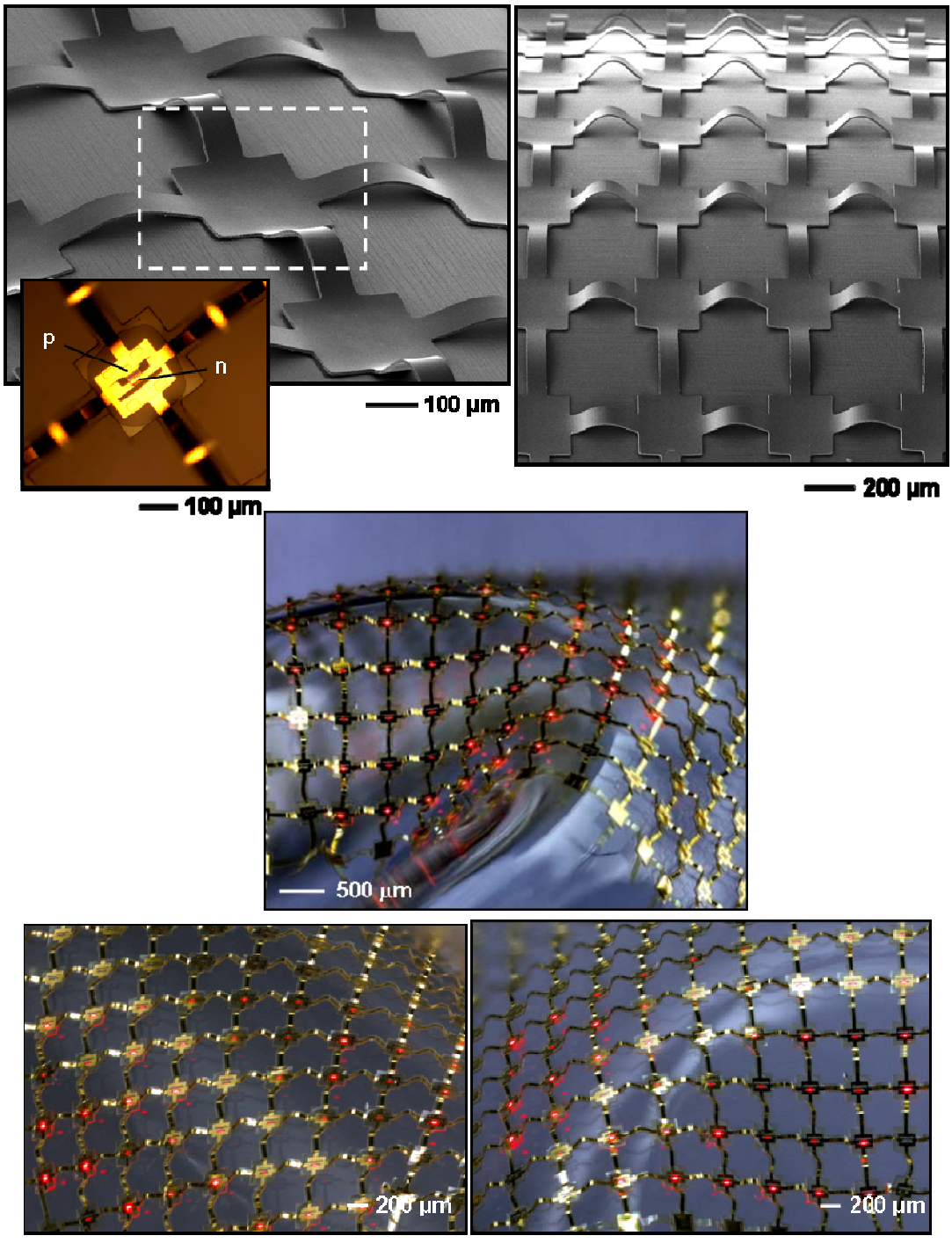


Figure 5.30 Optical microscope and SEM images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a bent/twisted rubber substrate.

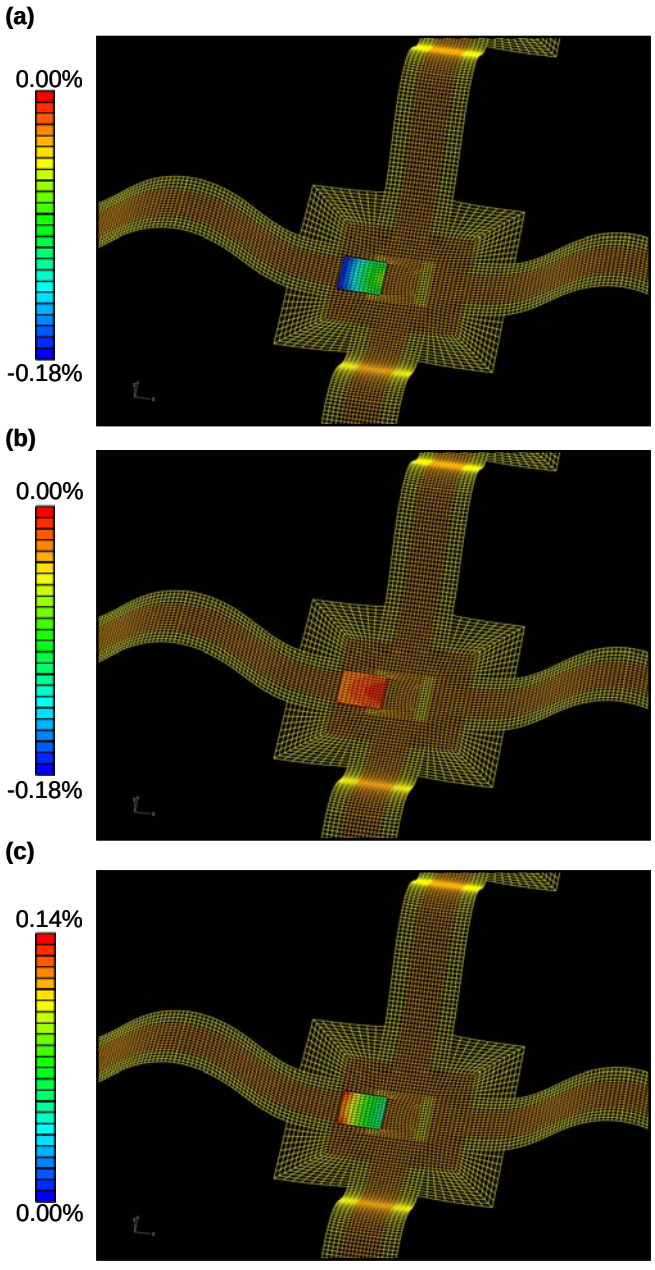


Figure 5.31 Strain distributions of a stretchable ILEDs display: (a) top surface, (b) middle surface (quantum well region), and (c) bottom surface of ILED.

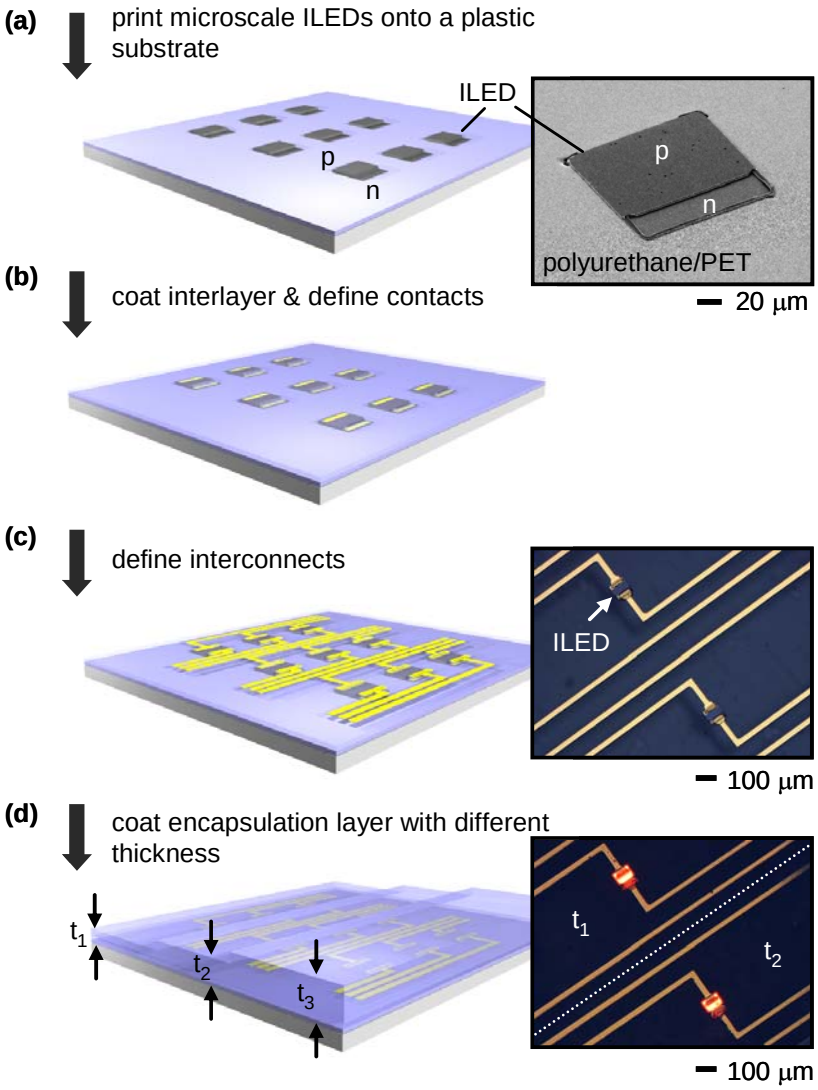


Figure 5.32 Schematic illustrations (left frames) of processing steps for fabricating bendable ILED systems with encapsulation layers of different thickness on a plastic substrate, and representative images (right frames). (a) Transfer printing delivers arrays of microscale ILEDs to a PET substrate coated with a polyurethane layer. Etching exposes the bottom, n-GaAs on one edge of each device. The SEM image on the right shows a individual ILED (~2.5 μm thick) partially embedded in the polyurethane layer on the PET substrate. (b) Coating and photopatterning a thin layer of epoxy on top of the devices and then depositing ohmic metals forms n and p contacts. (c) Photolithographic patterning establishes interconnection lines for electrical probing. (d) Coating and photopatterning defines encapsulation layers with different thicknesses in different regions. Optical micrographs of (c), (d) show top views of interconnected ILEDs in their off and on states, respectively. The top and bottom regions of frame (d) have encapsulation layer thicknesses of t_1 and t_2, respectively.

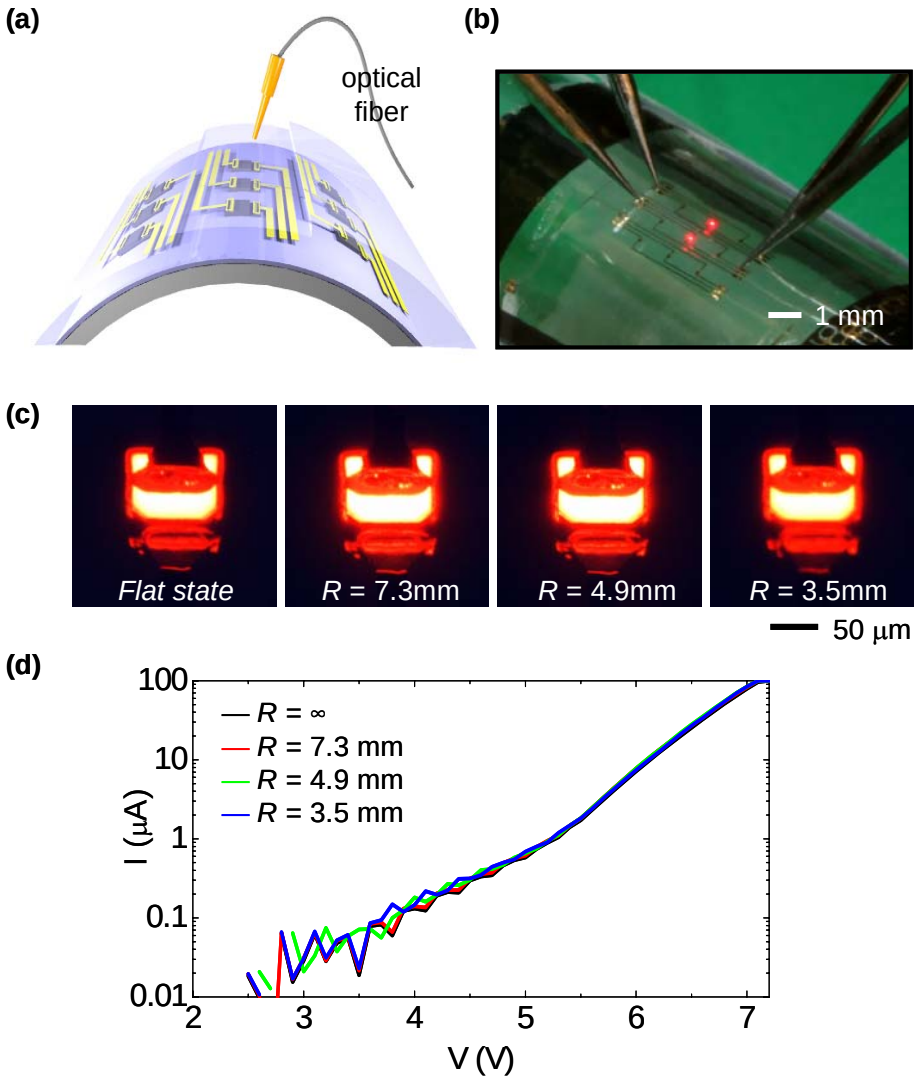


Figure 5.33 (a) Schematic illustration and (b) optical image of small, square ILEDs (100x100 μm, ~2.5 μm thick) formed on plastic substrate (PET, 50 μm thick) coated with polyurethane layer, in a bent configuration (R ~7.3 mm) during operation. (c) Optical micrographs of light emission from individual ILEDs at bending radii of ∞, 7.3, 4.9, and 3.5 mm, respectively. (d) Current (I) – voltage (V) measurements as a function of bending radius (∞, 7.3, 4.9, and 3.5 mm).

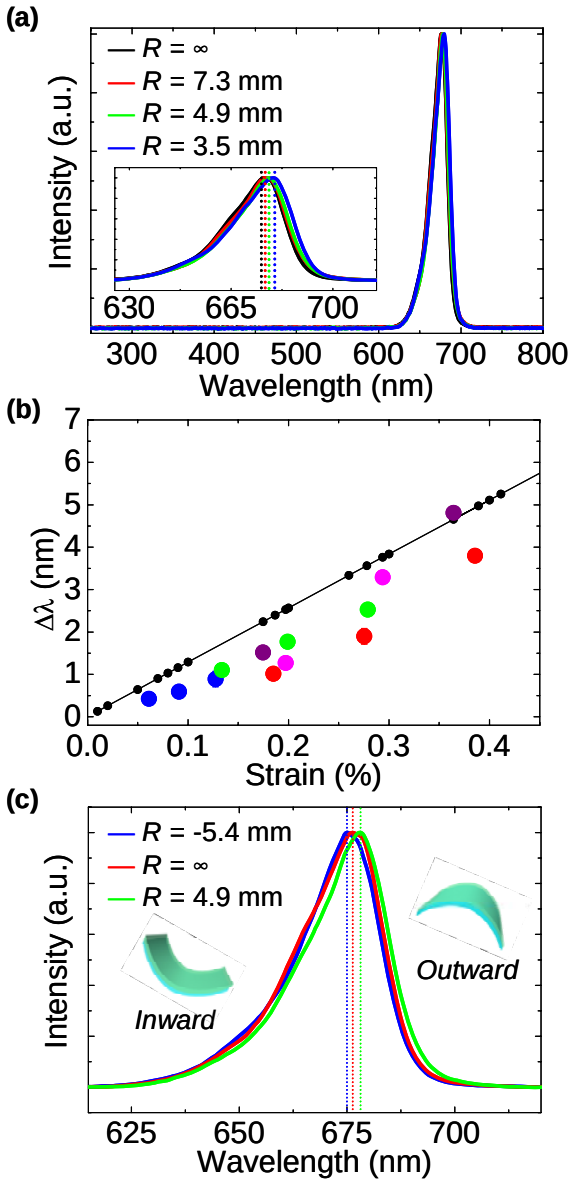


Figure 5.34 (a) Spectral characteristics of emission from ILEDs encapsulated with a ~5.5 μm thick layer of epoxy on a PET substrate (50 μm thick) at bend radii of ~ ∞, 7.3, 4.9, and 3.5 mm. The inset shows the same data plotted from 625 nm to 715 nm. (b) Change in the center wavelength of emission (Δλ) calculated (black) and experimentally measured (various colors) as a function of maximum uniaxial strain in the quantum wells of the ILEDs. (c) Emission spectra of an ILED in a flat state ($R \sim \infty$), during inward bending ($R \sim$ -5.4 mm), and outward bending ($R \sim$ 4.9 mm). The corresponding shifts in the emission wavelength are $\Delta\lambda \sim$-1.27 nm (inward) and $\Delta\lambda \sim$1.77 nm (outward).

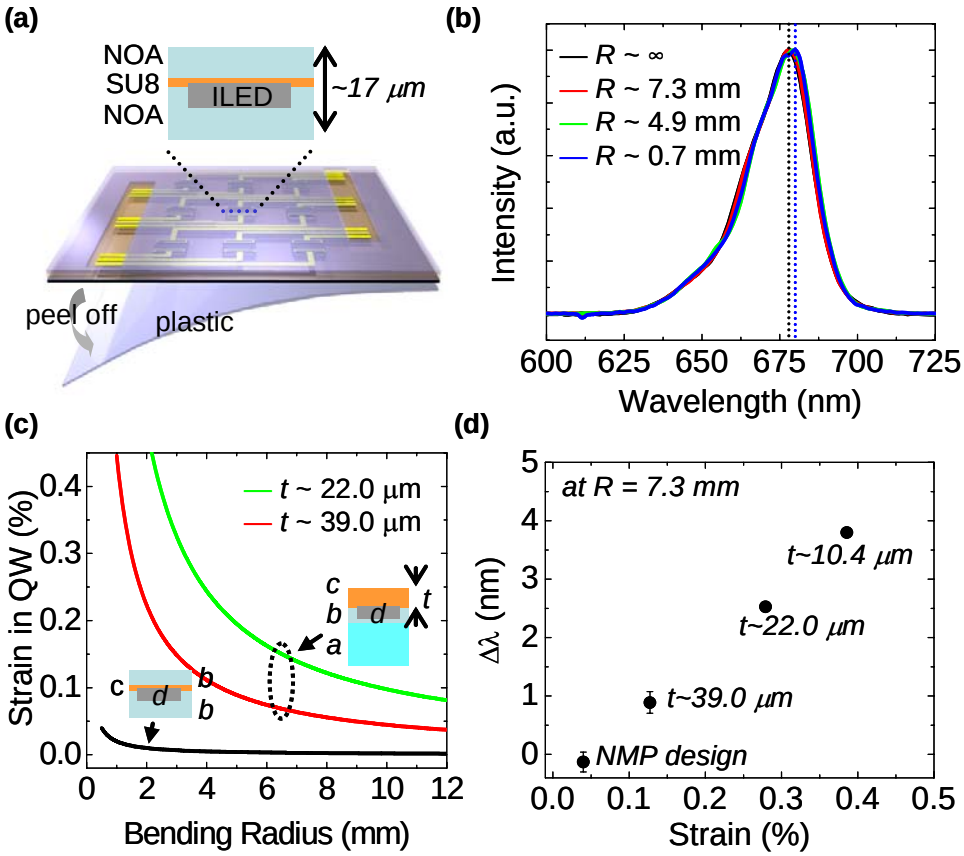


Figure 5.35 (a) Schematic illustration of an ILED system placed near the neutral mechanical plane, and with a total thickness of ~17 μm. Here, PET serves as a temporary substrate that is peeled away as a final step in the fabrication. (b) Spectral characteristics of emission of an ILED placed near the neutral mechanical plane, at bending radii of ∞, 7.3, 4.9, and 0.7 mm. The emission wavelength shifts by ~1 nm over this entire range. (c) Calculated maximum strain in the quantum wells of ILEDs encapsulated by epoxy (22.0 and 39.0 μm thick) on a PET substrate and in the neutral mechanical configuration of frame (a), as a function of bending radius. (d) Shift in the wavelength of emission for ILEDs encapsulated by epoxy (10.4, 22.0, and 39.0 μm thick) on PET substrate and in the neutral mechanical configuration of frame (a), in a bent state (R ~ 7.3 mm).

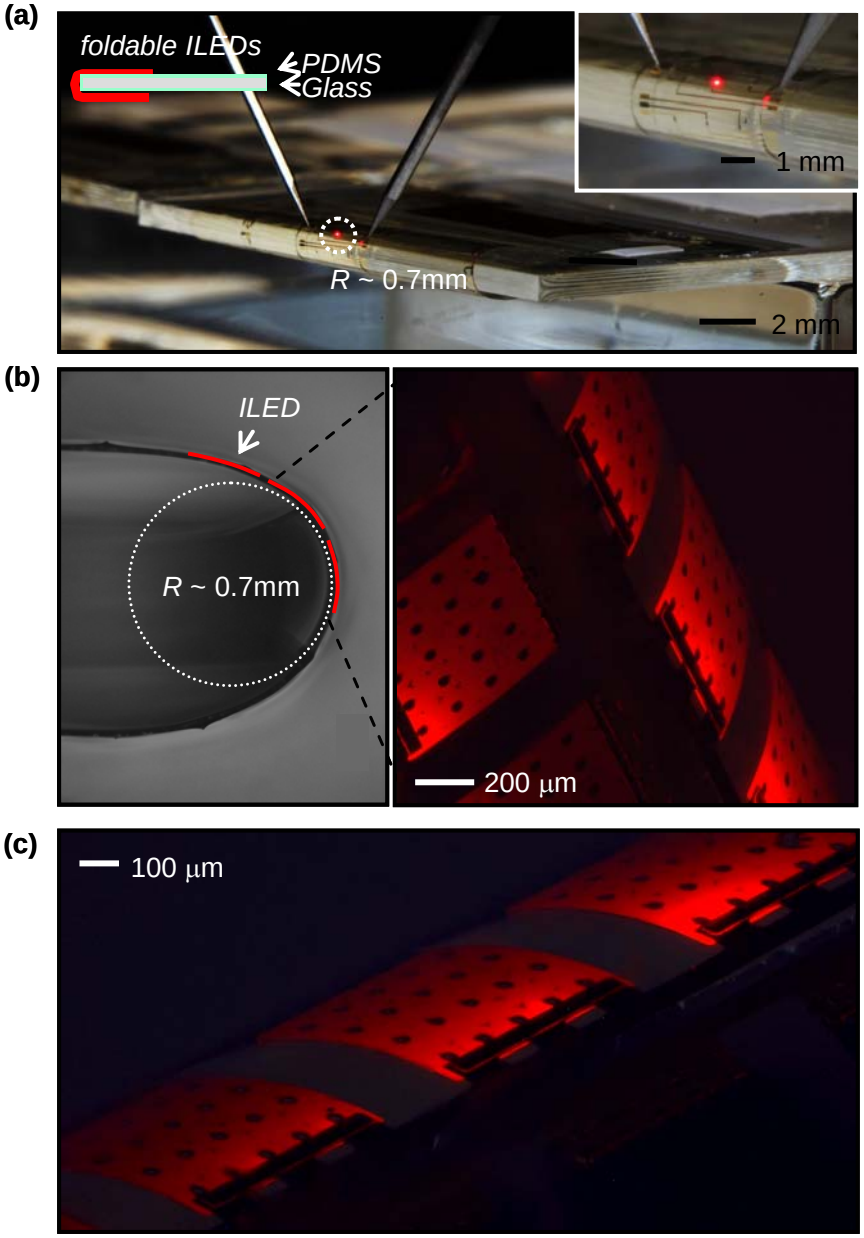


Figure 5.36 (a) Optical images of ILEDs (100x100 μm) in a neutral mechanical plane layout, during operation wrapped around the edge of a) a slide glass (1 mm thick). The bending radius is ~0.7 mm. (b) Cross sectional optical image of a similar ILED system and composite magnified view to show bending in the individual devices. (c) Similar composite image collected at a different viewing angle.

CHAPTER 6: SUMMARY

6.1 Summary

The results in chapter 2 and 3 presented that thin layers of silicon (Si) weakly bonded to plastic substrates exhibit three different failure modes at sufficiently high bending strains: cracking, slipping, and delamination, depending on the Si thickness. These failure modes are controlled by surface strain, interfacial shear stress, and interfacial normal stress, respectively. Experimental data agree well with analytical modeling based on beam theory [1]. The lateral dimensions (i.e. the lengths) of the Si ribbons are important on bending, as quantitatively verified by analytical modeling based on plate theory [1]. In particular, smaller regions of Si lead to more robust bending properties. The addition of encapsulating layers or neutral mechanical plane layouts can further improve bendability. These guidelines can be important for the design of flexible electronic systems that involve inorganic materials on plastic substrates.

As practical approach in flexible inorganic electronics, highly bendable array of the Si solar cells was demonstrated in chapter 4 [2]. Fundamental study of failures of inorganic materials on plastic substrate in chapter 2 and 3 enable optimized design for this bendable array of the Si solar cells. The types of solar cells module may create new possibilities for single crystalline Si photovoltaics, particularly in applications that benefit from thin, lightweight construction and mechanical flexibility.

As another approach in flexible inorganic electronics, the schemes reported in chapter 5 for creating ultrathin, microscale inorganic light-emitting diodes (ILEDs) and for integrating them into display and lighting devices create design options that are

unavailable with conventional procedures such as the planar thin-film processing. Therefore, flexible, stretchable, or deformable ILEDs lighting/display systems [3] were established by the use of these conventional procedures, based on fundamental studies related to behaviors of inorganic materials on plastic substrate in bending state. These studies also provide routes to flexible ILEDs with the capacity for bending to extremely small radii of curvature, i.e. foldable ILEDs. Careful analysis of the emission properties together with calculations of the bending mechanics and strain induced shifts in the bandgap give insights into the underlying physics and mechanics aspects. The results provide guidelines for the design of light sources with extreme levels of flexibility without losing optical properties. Additional research works, such as the design modification [4], new methods for interconnecting materials [5,6], the use of ultrathin sheets of substrates, or the use of low modulus materials, enable much higher degrees of stretchability and bendability beyond the degrees of them reported in my doctoral research. Further development of these systems continues at UIUC through the effort of other researchers in Prof. John A. Rogers research group.

6.2 References

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APPENDIX A: PROCESSING SCHEMES FOR VARIOUS INORGANIC OPTOELECTRONIC SYSTEM

The materials and methods for inorganic light-emitting diodes (ILEDs) lighting/display system, including epitaxial semiconductor multilayer design, polymeric anchor structures, large scale printing techniques, and electrical interconnection in direct or matrix addressable configurations, are described in this appendix in more details, for the flexible display, the large area display, the array of inorganic light emitting diode (ILED) devices with ultrasmall sizes/arbitrary shapes, the wavy ribbon devices, and the stretchable display. Significant components of appendix A were included in supporting online materials for "Printed Assemblies of Ultrathin, Microscale Inorganic Light Emitting Diodes for Deformable and Semitransparent Displays" published in *Science* **2009**, *325*, 977-981 by S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K.-C. Hwang, P. Ferreira, X. Li, K. Choquette, and J. A. Rogers [1].

A.1 Preparation of ILEDs

In this section, the sequence of processing steps used to retrieve ILEDs array appears below. Polymeric anchor structures support the ILEDs during undercut etching of the $Al_{0.96}Ga_{0.04}As$ sacrificial layer described in chapter 5.

A.1.1 Processing Scheme for Preparing ILEDs from a Source Wafer

A.1.1.1 Delineating the ILEDs

1. Clean an epi-stack ILED wafer chip (acetone, isopropyl alcohol (IPA), deionized (DI) water).

2. Deposit 800 nm SiO_2 by plasma enhanced chemical vapor deposition (plasma enhanced chemical vapor deposition (PECVD); PlasmaTherm SLR).

3. Pretreat with hexamethyldisilazane (HMDS) for 1 min.

4. Pattern photoresist (PR; Clariant AZ5214, 3000 rpm, 30 sec) with 365 nm optical lithography through an iron oxide mask (Karl Suss MJB3). Develop in aqueous base developer (Clariant AZ327 MIF) and bake on hot plate ($110\,^{o}C$, 3 min).

5. Etch oxide with buffered oxide etchant (BOE; Fisher, 130 sec).

6. Etch with an inductively coupled plasma reactive ion etcher (ICP-RIE; Unaxis SLR 770 System, 2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~21 min).

A.1.1.2 Undercut Etching of the ILEDs

7. Clean the processed wafer chip from step 6 above with HF (Fisher, 49%, diluted 10:1, 2 sec).

8. Pattern PR and bake at $110\,^{o}C$ for 5 min to form polymeric anchors at the corners of the μ-ILEDs.

9. Dip the wafer chip in diluted HF (Fisher, 49%, diluted 100:1) for an appropriate time (μ-ILEDs with 50 μm x 50 μm dimension: ~4 hrs, 100 μm x 100 μm: ~5.5 hrs) to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs. Rinse by-product using DI water at 1.5 hr intervals.

A.2 Device Fabrication

A.2.1 Processing Scheme for ILED Devices with Ultrasmall Sizes

Schematic illustration of these steps appears in Figure 5.11.

A.2.1.1 Preparing a Substrate with Metal Mesh

1. Deposit 300 nm SiO_2 with PECVD onto a silicon wafer

2. Pretreat surface with HMDS for 1 min, and then pattern PR.

3. Deposit 7/70 nm of Cr/Au by electron beam evaporation.

4. Lift-off PR in acetone to yield a pattern of Cr/Au in the geometry of a mesh.

5. Etch oxide with HF (49%, 38 sec).

6. Transfer print mesh to a glass substrate coated with poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning, spun at 600 rpm/5 sec, 3000 rpm/30 sec, cured in oven at $70\,^{o}C$ for 90 min) formed by mixing the base and curing agent with a ratio of 10:1 followed by thermal curing.

A.2.1.2 Printing the ILEDs

7. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 8.5:1.5, and then thermally cure.

8. Print ILEDs onto the glass substrate with Cr/Au mesh (n-contact).

9. Remove PR by washing in acetone.

A.2.1.3 Forming the Interlayer and P-contact Metallization

10. Spin coat the substrate from step 9 with a photodefinable epoxy (SU8-2, Microchem, spun at 1,500 rpm for 30 s). Soft bake at $65\,^{o}C$ and $95\,^{o}C$ for 1 min and 1.5min, respectively.

11. Pattern epoxy by exposing to ultraviolet (UV) light in a mask aligner for 14 sec, baking at $95\,^{o}C$ for 2 min, developing (SU8 developer, Microchem) for 15 sec, rising (IPA), and curing ($110\,^{o}C$, 35 min, slow cooling).

12. Pattern PR.

13. Deposit 7 nm of Pd-Au by sputtering.

14. Lift-off PR in acetone to leave a thin layer of Pd-Au on the top surfaces of the ILEDs (p-contact).

A.2.2 Processing Scheme for ILED Devices with Ohmic Contacts

A.2.2.1 Preparing the Substrate

1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water)

2. Expose to ultraviolet induced ozone (UVO) for 5 min.

3. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

A.2.2.2 Delineating the ILEDs

4. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

5. Deposit 800 nm SiO_2 with PECVD.

6. Pretreat with HMDS for 1 min.

7. Pattern PR and bake on hot plate ($110^{o}C$, 3 min).

8. Etch oxide with BOE (130 sec).

9. Etch with ICP-RIE (2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~16 min) to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs.

A.2.2.3 Forming a Passivation Layer and Undercut Etching

10. Clean the processed wafer chip from step 9 above (acetone, IPA, DI water).

11. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $110^{o}C$ each for 1 min and 1 min, respectively.

12. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing. The pattern includes a passivation structure to protect μ-ILEDs and an anchor structure to suspend ILEDs during the undercut etching.

13. Dip the wafer chip in diluted HF (49%, diluted 100:1) for ~2 hrs to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

A.2.2.4 Printing the ILEDs

14. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 10:1, followed by thermal curing. Contact 'inked' stamp against the substrate from step 13.

15. Retrieve the stamp after UV exposure (through the stamp) for 20 min. Cure the polyurethane layer by UV exposure for 2 hours.

A.2.2.5 Defining the N-contact Regions

16. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, ~12 min) to remove the epoxy on the top surface of the ILEDs.

17. Pattern PR and bake at $110\,^{o}C$ for 2 min.

18. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

19. Remove PR by washing in acetone.

A.2.2.6 Defining the N-ohmic Contact Metallization

20. Pattern PR.

21. Clean the surface of n-GaAs with HCl : DI water (1:1) for 30 sec.

22. Deposit 5/35/70 nm of Pd/Ge/Au by electron beam evaporation.

23. Lift-off PR in acetone to remain Pd/Ge/Au on the top surface of n-GaAs.

24. Anneal at $175\,^{o}C$ for 60min under N_2 ambient

A.2.2.7 Defining the P-ohmic Contact Metallization

25. Pattern PR.

26. Clean the surface of p-GaAs with HCl : DI water (1:1) for 30 sec.

27. Deposit 10/40/10/70 nm of Pt/Ti/Pt/Au by electron beam evaporation.

28. Lift-off PR in acetone to remain Pt/Ti/Pt/Au on the top surface of p-GaAs.

A.2.3 Processing Scheme for Flexible ILED Displays

A.2.3.1 Preparing the Substrate

1. Clean a glass slide (30 mm X 30 mm) (acetone, IPA, DI water).

2. Treat with ultraviolet induced ozone (UVO) for 5 min.

3. Spin coat with PDMS (spun at 600 rpm/5 sec, 3000 rpm/30 sec), formed by mixing the base curing agent with a ratio of 10:1.

4. Cure PDMS in an oven ($70\,^{o}C$, 90 min).

5. Clean a sheet of polyethylene terephthalate (PET; Grafix DURA-LAR, 32 mm X 32 mm X 50 μm) (IPA, DI water).

6. Laminate the PET sheet onto the PDMS coated glass slide, as a carrier for the following processing steps.

7. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

A.2.3.2 Printing the ILEDs

8. Liftoff an array of ILEDs (16x16 array of devices with dimensisons of 100μm x 100μm) using a flat PDMS stamp. Contact 'inked' stamp against the substrate from step 7.

9. Retrieve the stamp after UV exposure (through the stamp) for 20 min.

10. Remove PR by washing in acetone and then cure the polyurethane layer by UV exposure for 2 hours.

A.2.3.3 Defining the N-contact Regions

11. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 8 min) to remove the polyurethane layer covering the ILEDs.

12. Pattern PR and bake at 110^oC for 2 min.

13. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

14. Remove PR by washing in acetone.

A.2.3.4 Defining the N-contact Metallization

15. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65^oC and 110^oC each for 1 min and 1 min, respectively.

16. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

17. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

18. Pattern PR and bake at 110^oC for 2 min.

19. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant (Transene, Inc.).

20. Remove PR by washing in acetone.

A.2.3.5 Defining the P-contacts and P-contact Metallization

21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1 min, respectively.

22. Pattern epoxy by exposing to UV, developing, rising, and curing.

23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

24. Pattern PR and bake at $110^{o}C$ for 2 min.

25. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

26. Remove PR by washing in acetone.

A.2.3.6 Forming an Encapsulation Layer

27. Spin coat with epoxy (SU8-5, Microchem, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1.5min, respectively.

28. Pattern epoxy by exposing to UV for 14 sec, baking at $95^{o}C$ for 2 min, developing (SU8 developer) for 18 sec, rising (IPA), and curing ($110^{o}C$, 35 min, slow cooling)

A.2.4 Processing Scheme for Large Area ILEDs Displays

A.2.4.1 Preparing the Substrate

1. Clean a glass slide (50 mm X 50 mm) (acetone, IPA, DI water)

2. Deposit 50 nm of Ti by electron beam evaporation.

3. Pattern PR and bake on a hot plate ($110^{o}C$, 2 min) to form guide lines to assist in registration of ILEDs printed with an automated printer system.

4. Wet etch Ti with BOE (70 sec).

5. Remove PR by washing in acetone.

6. Expose to ultraviolet induced ozone (UVO) for 15 min.

7. Spin coat with PDMS (spun at 600 rpm/5 sec, 2500 rpm/30 sec) formed by mixing the base and curing agent with a ratio of 10:1.

8. Cure PDMS in an oven ($70\,^{o}C$, 90 min)

A.2.4.2 Printing the ILEDs

9. Selectively liftoff ILEDs (100µm x 100µm lateral dimensions) using a composite stamp in automated printing machine (fig. S3, S4) and print them onto the substrate from step 8, in a step and repeat fashion to form a 16x16 array.

10. Remove PR by washing in acetone.

A.2.4.3 Patterning the P-contact Metallization

11. Spin coat with epoxy (SU8-2, spun at 1,500 rpm for 30 s). Soft bake at $65\,^{o}C$ and $110\,^{o}C$ for 1 min and 1min, respectively.

12. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

13. Deposit 10/70 nm of Ti/Au by electron beam evaporation.

14. Pattern PR and bake at $110\,^{o}C$ for 2 min.

15. Wet etch Ti/Au with BOE and gold etchant for 35/20 sec.

16. Remove PR by washing in acetone.

17. Reactive ion etch (RIE, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs (fig. S8).

A.2.4.4 Defining the N-contact Regions

18. Pattern PR and bake at $110^{o}C$ for 2 min.

19. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

20. Remove PR by washing in acetone.

A.2.4.5 Patterning the N-contact Metallization

21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1 min, respectively.

22. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

24. Pattern PR and bake at $110^{o}C$ for 2 min.

25. Wet etch Ti/Au for 45/90 sec with BOE and Au etchant.

26. Remove PR by acetone rinse.

A.2.4.6 Defining the P-contact Regions and Metallization

27. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1 min, respectively.

28. Pattern epoxy with exposing UV, developing, rising, and curing.

29. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

30. Pattern PR and bake at $110^{o}C$ for 2 min.

31. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

32. Remove PR by acetone.

A.2.4.7 Forming an Encapsulation Layer

33. Spin coat with epoxy (SU8-5, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1.5min, respectively.

34. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

A.2.5 Processing Scheme for Stretchable ILEDs

Exploded view schematic illustration of the processing step appears in Figure 5.23.

A.2.5.1 Preparing Ribbon Shaped ILEDs

1. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

2. Pattern PR and bake for 2 min.

3. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 35 sec to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

4. Remove PR by washing in acetone.

A.2.5.2 Forming an Encapsulation Layer and Etching

5. Pattern PR on the top surface of the ribbons.

6. Deposit 3/15 nm of Ti/Au by electron beam evaporation.

7. Lift-off PR in acetone to remain Ti/Au on the top surface of the ribbons

8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65\,^{o}C$ and $95\,^{o}C$ for 1 min and 1.5min, respectively.

9. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

10. Dip the ILED in diluted HF (100:1) for 1 hr to release the ribbons from the wafer.

11. Rinse in DI water for 5 min.

12. Print ribbons onto a pre-strained substrate of PDMS with prepatterned metal lines.

A.2.6 Processing Scheme for Stretchable ILED Display

Schematic illustration of the processing steps appears in Figure 5.27.

A.2.6.1 Preparing the Carrier Substrate

1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water).

2. UVO treatment for 5 min.

3. Spin coat with PMMA (A2, Microchem, spun at 3,000rpm for 30 sec).

4. Anneal at $180\,^{o}C$ for 3 min.

5. Spin coat with polyimide (PI, poly(pyromellitic dianhydride-co-4,4′ -oxydianiline), amic acid solution, Sigma-Aldrich, spun at 4,000 rpm for 60 sec).

6. Anneal at $110\,^{o}C$ for 3 min and $150\,^{o}C$ for 10 min.

7. Anneal at $250\,^{o}C$ for 50 min in N_2 atmosphere.

8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1 min, respectively.

A.2.6.2 Printing the ILEDs

9. Liftoff ILEDs (16x16 array of devices with dimensions of 50 μm x 50 μm) using a flat PDMS stamp and contact the 'inked' stamp with the substrate from step 8.

10. Remove the stamp after UV exposure (through the stamp) for 60 sec and baking at $110^{o}C$ for 10 min.

11. Remove PR by washing with acetone. Fully cure the epoxy layer at $150^{o}C$ for 20 min.

A.2.6.3 Forming the Sidewall Region

12. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1 min, respectively.

13. Expose to UV for 14 sec and bake at $110^{o}C$ for 1 min.

14. Anneal at $150^{o}C$ for 20 min.

15. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs.

A.2.6.4 Defining the N-contact Regions

16. Pattern PR and bake at $110^{o}C$ for 5 min.

17. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

18. Remove PR by washing with acetone.

A.2.6.5 Defining the N- and P-contact Metallization

19. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65\,^{o}C$ and $95\,^{o}C$ for 1 min and 2 min, respectively.

20. Pattern epoxy by exposing to UV for 14 sec, developing for 15 sec, rising, and curing ($110\,^{o}C$, 35 min, slow cooling).

21. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

22. Pattern PR and bake at $110\,^{o}C$ for 2 min to define n-contact electrodes, designed as line patterns connected to n-GaAs, and p-contact electrodes, designed as line patterns that avoid crossing over the n-contact electrodes (fig. S16).

23. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

24. Remove PR by washing with acetone.

A.2.6.6 Interconnecting the P-contact Metallization

25. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65\,^{o}C$ and $95\,^{o}C$ for 1 min and 2min, respectively.

26. Pattern epoxy by exposing to UV, developing, rising, and curing.

27. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

28. Pattern PR and bake at $110\,^{o}C$ for 2 min.

29. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

30. Remove PR by washing with acetone.

A.2.6.7 Forming the Encapsulation Layer

31. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1.5min, respectively.

32. Pattern epoxy by exposing to UV, developing, rising, and curing.

A.2.6.8 Forming the Island/Bridge Structures

33. Deposit 150 nm SiO_2 by PECVD.

34. Pattern PR and bake at $110^{o}C$ for 2 min.

35. RIE (50 mTorr, CF_4/O_2 40/1.2 sccm, 150 W, 8 min) to etch SiO_2.

36. RIE (150 mTorr, O_2 20 sccm, 150 W, 50 min) to etch epoxy/PI layers.

37. Etch oxide with BOE (20 sec).

A.2.6.9 Transferring the Mesh

38. Immerse the ILEDs array mesh from step 37 in acetone ($80^{o}C$) for ~10 min to dissolve the PMMA.

39. Lift off the mesh using a PDMS stamp formed by mixing a base and agent with a ratio of 8.5:1.5.

40. Selectively deposit 5/30 nm of Ti/SiO_2 by electron beam evaporation on the bottom of island regions through a shadow mask.

41. Transfer the ILED mesh to a biaxially pre-strained PDMS substrate.

42. Anneal in an oven at $70\,^{o}C$ and release the strain.

A.3 References

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Sang Il Park was born on March 20, 1975, in Seoul, R.O.Korea. He attended Yonsei University, R.O. Korea for his undergraduate education in Materials Science and Engineering (MSE) and graduated with honors in 1998. He continued his studies for M.S. degree in MSE at Pohang University of Science and Technology (POSTECH), R.O.Korea from 1998 to 2000. At POSTECH, he received a M.S. degree with the study, Structural Evolution of ZnO/sapphire(001) Heteroepitaxy Studied by Real Time Synchrotron X-ray Scattering. In the same year, he joined Corporate R&D Center, Samsung SDI for a development of active matrix organic light-emitting devices (AMOLEDs) display. From 2000 to 2005, his major contributions are developments of the highest resolution 5.0" WVGA top emission AMOLEDs (2003) and the largest 17" UXGA full color AMOLEDs (2004) as a leader of process integration.

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